THE AMPSA DESIGN PHILOSOPHY

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1. INTRODUCTION

The Ampsa Amplifier Design Wizard (ADW) is the result of thirty years of intensive development. It is mainly used to design linear small-signal RF and microwave amplifiers and linear RF and microwave power amplifiers (The transistors used in the ADW are generally biased for class A, class AB or class B operation), but it also has useful oscillator analysis features. The impedance-matching capabilities provided [1] can be used for any application if the matching problem to be solved is known (load-pull data, etc.). Harmonic control features for high-efficiency amplifiers (class J [6], F, etc.) are also provided in the latest version.

Amplifier design with the ADW is a structured process. The stages in the amplifier are designed sequentially (stage after stage). Impedance-matching and/or modification networks (feedback and/or loading networks added to a transistor) may be designed for each stage. Extraction of the "real-frequency" impedances (and the gain) required for the synthesis of the matching or modification networks is based on constant power contours, constant gain circles and constant noise figure circles. The extraction is done in wizards and is automatic, but allows for user control. Optimization or optimization by re-synthesis is allowed at any stage during synthesis process and also when the basic design has been completed. This structured approach drastically improves the overall productivity of the design process. In addition to speeding up the process, it also leads to greater creativity and provides much more insight in the design than the standard optimization approach.

Power control in the Amplifier Design Wizard is based on an extension of the load-line approach commonly used at RF frequencies. By showing that it is actually the intrinsic load impedance that should be controlled and that the output power is inherently limited by clipping of either the intrinsic output voltage or the intrinsic output current in a transistor, Steve Cripps extended the usefulness of the RF load-line approach to microwave frequencies [6–7]. This approach was generalized in [2–3] by the introduction of the power parameters. These parameters map the intrinsic current and voltage of a transistor to the external voltages of the embedding circuit. This allows the intrinsic load line to be controlled (at the fundamental, as well as at harmonic frequencies) even when loading networks, impedance-matching networks or feedback is added to a transistor. The allowable load-line area on the intrinsic *I*/*V*-plane is also defined by four boundary lines, instead of only the maximum current and voltage. This provides a better approximation to reality and also introduces the option to control on which boundary the current of voltage clipping will start.

The networks designed with the Amplifier Design Wizard are practical and are adequate for surface-mount and chip-and-wire applications, as well as for MMICs. The networks could consist of transmission lines, single-layer parallel-plate capacitors, square-spiral inductors, bond wires and/or lumped components. Parasitic components can be specified for the lumped components and allowance is made for mounting pads too. The discontinuity effects associated with any transmission lines used are automatically compensated. The discontinuity models used

can also be customized to improve the accuracy in low-impedance circuits (high power) or at millimeter-wave frequencies.

The artwork for an ADW circuit is created automatically from the schematic. User-controllable constraints are built into the synthesis process to ensure that the artwork can be created for the networks synthesized, and that the microstrip performance will be close to the target electrical performance. The artwork of an ADW circuit can be refined by curving, bending or meandering selected lines. When this is done, the line lengths are adjusted automatically to keep the electrical design the same. Commands are also provided to modify stubs or to replace open-ended stubs with equivalent main-line sections. The schematic can also be refined on completion of a synthesis step. Inductors can be replaced with hair-pin inductors, bond wires (single or double bond wires are allowed), square spiral inductors or solenoidal coils, while capacitors can be replaced with single-layer parallel-plate capacitors or overlay capacitors. If necessary, the circuit as designed up to that point can be optimized to restore the target performance before proceeding with the synthesis process.

Impedance-matching network synthesis is based on the transformation-Q approach outlined in [1–3]. "Real-frequency" specifications [8] are used to define the matching problem to be solved. The transducer power gain of the matching network in the passband, and the source or load reactance at harmonic frequencies (narrowband networks), can be controlled. Lumped, distributed and mixed lumped/distributed matching networks can be synthesized. Pads and parasitic components can also be specified for the lumped elements and are taken into account in the synthesis process. Multiple solutions are provided to each matching problem solved. The sensitivity of each network presented is also evaluated and serves as a guide to the designer in selecting the best solution to the matching problem.

The synthesis of the modification networks (feedback and/or frequency-selective resistive loading networks) is based on extensions of [9]. These networks are essential in most amplifiers and serve to level the gain, provide the degree of stability required and reduce the gain-bandwidth constraints of the matching problems to be solved. It is useful to view adding modification sections to a transistor as a pre-conditioning step before the associated matching problems are solved.

The Amplifier Design Wizard is typically used as a front-end to one of the general-purpose microwave circuit simulators available on the market. The ADW artwork can currently be exported as Microwave Office™ scripts, as native Sonnet Software® files or in DXF format. A CST Microwave Studio™ technology file is also created when the artwork is exported in DXF format. This allows for extruding the DXF layers at the required elevation with the required thickness in Microwave Studio™. Footprints are also created for any bond wires used (the actual bond wire is not created yet).

The amplifiers designed with the Amplifier Design Wizard are usually good enough to only require fine tuning in a general-purpose simulator. This applies to class A, as well as class AB and class B amplifiers when the 2nd harmonic intrinsic output voltage can be neglected. (It should be noted that the optimum fundamental frequency power load line for a class B stage is generally very similar to that of a class A stage at the same DC operating point.) The matching networks for high-efficiency amplifiers (like Class F and continuous class F amplifiers [10], as well as Doherty amplifiers [11]) can also be designed in the ADW, but the simulation of the amplifier must be done externally. Depending on the design, measured or simulated load-pull data may be required to define the associated matching problems.

2. POWER CAPABILITY

An important power feature in the Amplifier Design Wizard is that non-linear transistor models are not used in it. (A non-linear model may be used in another tool to generate the *S*-parameter, noise parameter and/or load-pull data required in the ADW.) In order to control the power performance, linear models must be fitted to the *S*-parameter and the noise-parameter data associated with the desired DC operating points (not necessarily the bias point) of the different transistors used. The required models can be fitted in the Device-Modification section of the Amplifier Design Wizard. Initialization and optimization features are provided for this purpose. The *S*-parameters associated with the model should fit the measured data tightly.

I/*V*-curve boundary lines must also be specified for each transistor used. These define boundaries on the fundamental tone intrinsic output current and voltage of each transistor. The parameters of the *I*/*V*-curve boundary lines can be established by using measured dynamic (preferable) or static *I*/*V*-curve measurements. When *I*/*V*-curve data is not available, the relevant parameters can be estimated and adjusted based on any power data information (like P_{1dB}) available.

Power parameters [2–3] are used to estimate the maximum linear output power (output power just before the onset of clipping of the intrinsic output current and/or voltage) obtainable from each transistor. The optimum power terminations for the (modified) transistor can be calculated and displayed. Contours of constant maximum linear output power can also be displayed with the optimum terminations. Ideally, the optimum power terminations should be compared with actual load-pull measurements to ensure that the model extracted is adequate. Note that in GaAs FETs and bipolar transistors, the maximum linear output power usually corresponds closely to the 1dB compression point (P_{1dB}).

When the power performance of a multi-stage amplifier is calculated, the influence of each transistor on the power performance is established. This is done by assuming that clipping occurs in only one transistor at a time, with the other transistors ideal. The output power of each stage is referenced to the load. (That is, the output power is increased with the operating power gain of the stages between the transistor of interest and the actual load termination.)

Note that power margins can be specified for the driver stages during optimization. This will ensure that the output power will be limited mainly by the load stage. The power of each stage can also be controlled to be higher than a target level, or to be within a target window. The latter option is important when the output power is required to be constant over frequency (limiting amplifiers).

An estimate of the difference between the maximum linear output power and the saturated output power can also be specified for each transistor when the model is created. This specification is used with the small-signal gain to define a saturation curve [4]. This saturation curve is used to estimate the actual output power and the compression depth of each transistor for a given level of the input signal. This feature allows for establishing proper power levels at the different points in the amplifier chain, and is also useful to ensure that a transistor in the amplifier chain is not overdriven. It also allows for indirect control over the harmonic and inter-modulation distortion generated.

All of these power features allow for fast simulation and optimization of cascade amplifiers with several stages. It also allows power amplifiers to be designed when non-linear

transistor models are not available yet. It should also be noted that non-linear models are not always very accurate and better results may be obtained with the ADW approach.

3. THE CONVENTIONAL APPROACH TO DESIGNING RF AND MICROWAVE CIRCUITS

The prevalent approach to the design of RF and microwave circuits today is still the optimization approach. An initial solution is obtained by some means or other, and this solution is "optimized" (improved by using optimization techniques) with a general-purpose RF and microwave circuit simulator. This approach has the following disadvantages:

- The optimization as provided in most circuit simulators is limited to a specific pre-defined topology.

- A circuit (amplifier) is usually optimized as a whole. It is not systematically put together (synthesized) in a step by step process.

- In some cases, a single-frequency circuit is synthesized systematically for use as the initial solution in a broadband design, but there is no guarantee that the specific circuit chosen is the optimum, or even a good choice, for the wide-band problem.

- Optimization problems are subject to the phenomenon of local minima and, therefore, the initial values assigned to the components. Even with a fixed topology, the chances of finding the global optimum to a practical, non-trivial microwave optimization problem are often poor.

- The optimum targets for the problem to be optimized are usually not known, at least not initially.

- Because only a single solution is optimized, no perspective is obtained on the problem solved.

While this approach is certainly workable, it is slow, depends heavily on the experience of the designer (or some other source), and usually yields inferior results. The requirement of initial solutions is also a major drawback.

4. DESIGNING CIRCUITS BY DOING SYNTHESIS-BASED SYSTEMATIC SEARCHES

In the ADW the basic point of departure is that one cannot rely only on optimization techniques to find close-to-optimum solutions. A solution to this problem is to find solutions by doing

systematic searches. A simple grid search is, however, not the answer. In order to do the required search efficiently, the search must, in the first place, be done on the correct parameters and, secondly, it should be synthesis based. A number of the best solutions found in the systematic search are then optimized, after which the user can choose the best solution from the potential solutions presented.

Note that the systematic searches also eliminate the initialization problem.

4.1 IMPEDANCE MATCHING WITH THE ADW

When impedance-matching networks are synthesized, the transformation *Q*s, as defined in [1–3], were found to be excellent parameters for a systematic search. Similar to the *Q* of a circuit, these *Q*s are inherently constrained in range, and the step size can be chosen realistically without significantly reducing the probability of finding close-to-optimum solutions. The last two transformation *Q*s in a network are constrained further by synthesizing the network to approximate the specified gain at, at least, one of the frequencies in the passband (a gain window is set for this purpose). The efficiency of the search can also be increased by doing a coarser main search combined with finer searches around a number of the best solutions (usually 10 to 25) obtained in the main search. The best solutions obtained are then optimized with a steepest-gradient optimization routine (random optimization is, in principle, not used).

It is important to realize that the searches done are topology independent. It is, however, a simple matter to constrain the search on the transformation *Q*s to result in a wide variety of practical topology constraints. Some of the constraints which are allowed in the ADW are to limit solutions to:

- Low-pass form.
- High-pass form.
- Networks without any series capacitors.
- Networks without any shunt inductors.
- Networks suitable for interstage biasing purposes (4 or more elements are required).

Constraints on the characteristic impedances, the line lengths and the values of any lumped components were also implemented. The option to replace shunt capacitors with shunt overlay capacitors is also provided.

The impedance-matching modules can synthesize

- Lumped-element matching networks.
- Commensurate distributed matching networks (The line lengths are fixed and the line widths are used as variables).
- Non-commensurate distributed matching networks (The line widths are fixed and the line lengths are used as variables).
- Mixed lumped/distributed matching networks (Lumped elements are used to minimize the line lengths).

Note that the commensurate matching algorithm implemented was generalized so that different lengths can be used for the main-line sections, the open-ended stubs and the short-circuited stubs. By using short stubs, the option to replace any stub with an equivalent stub, or a lumped component with pads, is introduced (if the line length is short, the tangent function is essentially linear).

Matching networks for power transistors are often designed without using any stubs. When non-commensurate impedance-matching networks are synthesized this can be done by using the following options:

- Choose the topology option not to have any shunt inductors (short-circuited stubs).
- Choose the option to replace any open-ended stubs with double stubs.
- Choose the option to replace double stubs with stepped main-line sections.

When commensurate impedance-matching network are synthesized, the low-pass option can be used, and the line length to be used for open-ended stubs can be set to be very short. The constraints on the allowable widths of these stubs should be set to force the stubs to be narrow. Note that a schematic command to transform an open-ended stub to a stepped main-line section is provided in the Analysis Module, with various other transformation options.

When mixed lumped/distributed matching networks are synthesized, the line lengths are reduced by using lumped elements. Constraints can also be imposed on the values of the lumped elements. (From the viewpoint of accuracy, a short line or stub is preferable to a lumped component.) The pad size to be used with each type of lumped component (series or shunt capacitors, or series or shunt inductors) must be specified by the user. In order to minimize the parasitic effects introduced, any pads specified should be as small as possible.

All of the matching networks are synthesized to approximate the specified transducer power gain versus frequency response between two specified complex terminations. The specifications must be made in “real-frequency” format (terminations and gain specified at a number of frequencies in the passband of interest). No equivalent circuits or an analytical expression for the gain response is required, or used. The gain at each frequency can be specified to be less than, greater than or equal to the gain value specified. The less than option is useful when rejection is required.

In order to evaluate the relative sensitivity of the different solutions to component changes, a worst-case tolerance analysis is done on each network in the results section of the relevant impedance matching module. The default tolerance value is 1%.

The choice of the specific solution to be used is left to the user. Having several solutions to choose from (different topologies and different element values) is an advantage from a manufacturing viewpoint and also provides perspective on the problem being solved.

The option to create an ADW circuit file for the solution chosen, or to insert the solution chosen at a marked position in a previously created circuit file, is provided in the results section of the impedance-matching module.

Microstrip capability

The ADW synthesizes networks electrically, that is, in terms of inductance, capacitance, resistance, characteristic impedance and electrical line length. If microstrip or stripline solutions

are required, these electrical solutions must be transformed and optimized before they are of practical use. A distributed ADW circuit can be transformed automatically into microstrip or stripline form, with the option to adjust the line lengths to compensate for the shifts in the reference planes caused by step, tee and cross junction discontinuities. Step junctions can also be tapered to reduce the associated discontinuity effects. If suitable values were chosen for the characteristic impedances and line lengths, the performance of the transformed circuit usually corresponds closely to that of the original circuit, even when complete amplifier circuits are transformed.

Note that the characteristic impedances should be chosen to minimize any transformer effects or reactive loading effects at the different junctions. The information required to make an appropriate choice is provided when required. It should be realized that the discontinuity effects decrease as the substrate height is decreased. However, when lines are too narrow, the conductor losses will be unacceptable.

An ADW circuit can be exported in Super Compact™ or Touchstone™ netlist format, or as a Microwave Office™ script (This script can be run in Microwave Office™ to create the schematic and the associated artwork). Native Sonnet Software® files (planar EM simulation) can also be created for the ADW artwork.

DXF files can also be exported by the ADW and these can be imported into an EM simulator. Many features were implemented to simplify the process of exporting the ADW artwork to CST's Microwave Studio™ (3D EM simulator). Note that a CST technology file is also created when the ADW artwork is exported in DXF format. This technology file is used in Microwave Studio™ to extrude each DXF layer at the correct elevation with the correct height. Layer mapping is allowed in the ADW for single-layer capacitors, bond wires and vias, for different substrates and also for mounting transistor dies on ridges (chip-and-wire applications). Overlay capacitors with a centered via, or with a single or two offset vias, are also allowed.

The ADW has been set up to handle chip-and-wire circuits, as well as basic MMIC circuits well. Single or double metallization, air-bridges, a capacitor dielectric layer and vias can be used when MMIC circuits are designed in the ADW. Models for single-layer capacitors, square spiral inductors, single and double bond wires and solenoidal coils are also provided. The parameters in these models can be optimized by using a 2D or 3D EM simulator.

If the circuit or sub-circuit exported is optimized externally, the two-port parameters of the optimized network can be imported into the ADW (Touchstone™ "*.s2p" format). This approach is also followed when circuits are realized on media other than microstrip or stripline (co-planar, suspended substrate or waveguide circuits are not yet supported in the ADW). Similarly, any components not presently supported in the ADW (like radial stubs, interdigital capacitors, circular spiral inductors, etc.) can be designed with another software tool, after which the associated *S*-parameters (and noise parameters) can be imported into the ADW.

Note that an ADW circuit can be exported in electrical or geometrical format. The electrical circuit description can be used as target for any external microstrip/stripline optimization required. Depending on the substrate height and the impedance levels, ADW microstrip or stripline circuits are usually adequate up to at least 12GHz. However, customization features were implemented to allow accurate results even at millimeter-wave frequencies, and also for low-impedance power amplifier circuits. These features are available in the professional version of the ADW.

The Equivalent Passive Problem

The best way to synthesize an amplifier is to control the available power gain and the noise figure, or the operating power gain and the output power, of each stage in the amplifier. The design cycle should be started at the source side when a low-noise amplifier is designed and at the load side when a power amplifier is designed. When a high-dynamic range amplifier is designed, the low noise section and the power section can be designed separately and can then be joined by using an interstage matching network.

If this approach is followed, the input port or the output port of each (modified) transistor used must be terminated in an impedance which lies on or near to the circumference of the target constant gain circle or constant noise figure circle or constant power contour, at each frequency of interest. An impedance-matching network must, therefore, be synthesized to transform the existing impedances at the port considered to those required at the different frequencies of interest.

If the transistor is inherently stable or was compensated to be so [1–3], it is possible to transform each of the circle problems (constant gain or constant noise figure circles) to a passive impedance-matching problem which is exactly equivalent (Inherent stability is not required when the noise figure is controlled). To understand how this is possible, it is only necessary to realize that the problem of matching a passive source to a passive load is also a circle problem when the required transducer power gain is less than unity [1–3]. The active problem, therefore, reduces to finding the passive problem for which the circle required is exactly the same as the target constant noise figure or constant gain circle, at each frequency of interest.

In those cases where inherent stability was not established or when the output power is controlled (elliptic contours), the optimum point on the relevant circle or power contour can be selected to complete the specifications for the equivalent passive problem. The option to enforce such a “point-match” is also provided in the inherently stable case. Note that, when a “circle-match” is possible, a point-match should only be enforced if the performance is only acceptable over a small segment of the relevant circle.

The option to optimize the matching networks synthesized to provide a better fit to the targeted active performance is provided in the results section of the Impedance-Matching Module.

4.2 DEVICE MODIFICATION

The capability to solve impedance-matching problems and the concept of the equivalent passive problem are critical factors in establishing a general amplifier synthesis capability. However, it will be found that these alone do not bring one very far. The following problems, all of which are associated with the transistor(s) to be used, still need to be solved:

- Stability outside the passband can be a major problem. Synthesizing a network that will provide the required performance inside the passband and that will ensure stability outside the passband can be difficult. When it can be done, unnecessary constraints are imposed on the performance inside the passband.

- All non-trivial impedance-matching problems have inherent gain-bandwidth constraints. If these constraints are too severe and cannot be reduced, the bandwidth can only be increased by degrading the associated VSWR (that is, when a lossless matching network is used).

- Transistors have inherent gain slopes at higher frequencies. While these gain slopes can be removed with lossless networks with suitable positive slopes, the sensitivity to any variation in the component values is frequently a problem.

- The optimum noise figure or optimum power termination for a transistor is usually very different from the optimum gain termination.

The answer to these problems is to add frequency-selective, resistive, feedback and/or loading networks to the transistor. In doing so, the transistor is modified to be more suitable to the application at hand. These networks will be referred to as device modification networks, and each resistive section will be referred to as a modification section. Two series of modification techniques were originally developed. Only the double-section modification technique is implemented in recent versions of the ADW. The main reason for this is that a single modification section rarely provides the performance required, and when it is the best option, the best double-section network will effectively reduce to a single section.

4.2.1 GAIN SLOPE CONTROL WITH LOSSY SECTIONS

In the first series of modification techniques developed, a table of the components required to provide a specified slope in the maximum available power gain (MAG) or the maximum stable power gain (MSG) is created. (To understand why the MAG is targeted, is it necessary to understand that a flat gain response and low input and output VSWRs can only be obtained with lossless matching networks if the MAG of the transistor has been leveled first). Tables can be created for

- Voltage-shunt feedback sections
- Current-series feedback sections
- Shunt loading sections
- Series loading sections

In each case, the gain slope is controlled with a resistor used in combination with some lossless component(s). (In the simplest case, a resistor is used in parallel with a capacitor or in series with an inductor). By using a resistive network to reduce the gain slope, the stability and the VSWRs may be improved simultaneously. In general, sensitivity is also not a problem. This follows because these networks usually have Qs which are low in comparison with those required from an equivalent lossless network.

Note that the MSG can only be controlled with a feedback section. If the slope in the MAG is set to be equal to that in the MSG, tables of the components required to just stabilize the transistor at different gain levels can be created.

Different gain-slope control sections can be combined sequentially. Some fraction of the gain slope can first be removed with one section, after which a second section can be used to level the gain. The first section can be used to control the MSG or the MAG, while the second is usually used to level the MAG. Note that if feedback sections, as well as loading sections are used, the feedback must be applied before the loading.

Better VSWRs can often be obtained when two sections are combined to reduce, or to level, the slope in the MAG. At least two modification sections are usually required for good results.

4.2.2 THE DOUBLE-SECTION MODIFICATION TECHNIQUES

In the second series of modification techniques any two of the different modification sections (voltage-shunt feedback, current-series feedback, shunt loading and series loading) are combined automatically to level the gain of the stage synthesized. While only the MAG or the MSG could be controlled with one of the single-section modification networks, any of the following gain functions can be controlled with a double-section modification network:

- The MAG.
- The MSG.
- The transducer power gain (G_T).
- The available power gain (G_a).
- The operating power gain (G_w).
- The available power gain associated with the optimum noise figure of the modified transistor ($G_{a\text{opt}}$).

Note that the performance of any stages synthesized previously (multistage amplifier) are taken into account when the gain is controlled in the ADW.

The networks synthesized are optimized first before the solutions are presented to the user. Optimization is in terms of an error function, through which control is provided over the following parameters:

- The average power gain over the passband.
- The gain ripple over the passband.
- The highest input VSWR and output VSWR in the passband.
- The highest noise figure in the passband.
- The degree of difficulty of the noise match, expressed as a VSWR.
- The lowest Rollette stability factor in the passband or over the complete frequency range over which *S*-parameter data were provided for the transistor.

- The load and source stability factors (LSF and SSF; these factors are generalizations of μ and μ-prime [5]).
- The maximum linear output power. The output power can be optimized to be higher than a critical level or to be within set boundaries.

Note that the VSWRs targeted could be actual VSWRs (like the final input VSWRs) or could be VSWRs used to indicate the degree of difficulty of the impedance-matching problem to be solved. To appreciate this, consider the case where the MAG is controlled. If perfect matching networks could be designed, the input VSWRs, as well as the output VSWRs, would be unity when the matching networks are in place. In the ADW, the poorest VSWR in the passband before a matching network is added to a circuit is used as an indication of the degree of difficulty of the associated matching problem. The VSWR is calculated in terms of the actual complex source or load impedance in place (Z_0) before the matching network is added.

It is important to realize that when the MAG, G_a, G_w or G_{anopt} is controlled, a conjugate match at the other port of the modified transistor is implied. This implies that a matching network is required at that port before the performance targeted can be realized. No matching networks are required when the transducer power gain (G_T) is controlled. When $G_{an\mathrm{opt}}$ is controlled, an optimum noise match is required on the input side and a conjugate match on the output side.

Contrary to popular believe, excellent low-noise stages can usually be synthesized by using resistive sections. Such sections should, however, be used on the output side of the transistor. The best low-noise results are usually obtained by synthesizing the modification section to control G_{anopt} or the MAG. Similarly, modification networks are usually added on the input side of the transistor when the output power should be maximized.

Similar to impedance-matching networks, the double-section modification networks are synthesized by doing a synthesized-based systematic search. The search is done over all networks which will provide the specified gain and input or output VSWR, at at least one of the passband frequencies. A number of the best solutions (up to 45) are stored and optimized with a steepest-gradient optimization technique. The search can be global, can be constrained to not include some modification sections (like voltage-shunt or current-series feedback, or resistive loading on the input or output side), or it can be done for a specific modification section. As in the case of impedance matching networks, the choice of the specific modification network to be used is left to the user.

In earlier versions of the ADW, no provision was made for connecting lines or for the pads required for the lumped components when modification networks were synthesized. This was found to be a major drawback and was corrected by adding an optimization phase to the synthesis cycle. Because of the optimization step, one-port parasitic components are also allowed for the lumped components. Note that unaccounted parasitic effects and phase shifts can have a disastrous effect on the expected performance of a voltage-shunt feedback loop.

5. STABILITY CONSIDERATIONS

A complete picture of the relative stability of a (modified) transistor is not provided by the k factor (Rollette stability factor) typically used. One of the reasons for this is that small changes inside the circuit can cause large changes in k. It has been found that the loop gain associated with each feedback loop should be evaluated too. Although the loop gain is dependent on the terminations used, it provides the information and the control required to handle most stability problems. The loop gain of a circuit can be evaluated in the Analysis Module of the ADW. Reflection analysis features are also provided in the Analysis Module.

Note that ignoring the information provided by the k factor is not advocated.

Any potentially unstable two-port ($k < 1$) can be stabilized by loading its input and/or output terminals with series or shunt resistance (Loading on both sides is sometimes required). Stabilization is sometimes also possible with a voltage-shunt feedback resistor. Valuable insight into the degree of instability is often gained from the values of the stabilizing resistance required. Tables of the resistance required are, therefore, provided in the Device-Modification Module and in the Analysis Module.

The performance loss associated with inherent stability can sometimes not be tolerated. When conditional stability is sufficient, the μ and μ-prime stability factors [5] are useful. These factors can be used to establish the change in the load termination (μ) or the source termination μ-prime (expressed as VSWRs), that can be tolerated before oscillations become possible (That is, oscillations will not be possible as long as the VSWRs are smaller than some value). They work well when the circuit terminations are purely resistive and only lossless elements are used to connect the terminations to the transistor. The load stability factor (*LSF*) and the source stability factor (*SSF*) used in the ADW are generalizations of μ and μ-prime. They allow calculation of the VSWRs that can be tolerated before oscillations become possible in terms of any arbitrary termination (and, therefore, also the actual termination) at the transistor port of interest.

When they are calculated for a complete circuit with purely resistive terminations, the *LSF* and *SSF* values calculated are equal to μ and μ-prime, respectively.

6. THE CIRCLE AND POWER MODULES

The impedance-matching module of the ADW was developed to synthesize solutions to passive impedance-matching problems. Active matching problems are converted to equivalent passive impedance-matching problems when the ADW CIR or CIL Wizards are used. Any one of the following parameters can be set as target in these wizards:

- The operating power gain (G_w).
- The available power gain (G_a).
- The transducer power gain (G_T).
- The noise figure (F).
- The maximum linear output power (P_{out}).
- The effective maximum linear output power (P_{out}-P_{in}).

The specifications set for the stage designed correspond to one of the following:

- A set of constant gain circles.
- A set of constant noise figure circles.
- A set of constant maximum linear output power (P_{out}) or effective maximum linear output power (P_{out}-P_{in}) contours.

A Summary Table is displayed directly after the specifications for the performance required are made. It summarizes the potential performance on the circles or contours targeted. The variation of the best and the worst performance on each circle or contour, over the passband of interest, is also displayed. Note that the circles or contours of interest can be displayed graphically too.

The option to allow a circle match or to force a point match, at each of the passband frequencies of interest, should be made after selecting the circles or contours to be used. If a point match is required, the optimum point on the relevant circle or contour must be selected. The default optimum point is selected by using an error function. The parameters of this error function can be modified by the user when the Summary Table is displayed.

To allow evaluation of the performance around each circle or contour, a table listing the performance at different angles around the circle or contour is displayed. Zoom capabilities are provided in these tables in order to allow displaying of the performance at any point on the circle or contour of interest. The optimum point on the circle or contour is high-lighted in the table.

The following parameters are listed in these tables:

- The power gain (G_a, G_w or G_T) on a constant noise figure circle or a constant output power contour, or the noise figure (F) around a constant gain circle or a constant output power contour. When the operating power gain (G_w) or the output power (P_{out}) is controlled, the noise figure associated with a conjugate match on the input side, or with the termination currently in place on the input side, is calculated.

- The degree of difficulty of the associated impedance-matching problem expressed as a VSWR. The required impedance is compared with the impedance actually in place when this is done.

- The Sterne stability factor with the stabilizing influence of the terminations taken into account.

- The tunability factor is a measure of the influence that any impedance changes (tuning) on the output or input side of the transistor will have on the impedance at the other side. When the input and the output sides of a transistor are perfectly isolated (unilateral case), the tunability factor is zero. A tunability factor of less than 0.3 is usually acceptable. Note that poor tunability can be an advantage when the input VSWR of a low-noise stage or the output VSWR of a power stage is controlled by the termination on the other side of the (modified) transistor (indirect VSWR control via s_{12}).

- Worst-case sensitivity factors associated with variations in the controlling admittance. A default tolerance of 1% in the controlling admittance is assumed when these sensitivity factors are calculated. Sensitivity factors are calculated for the noise figure (δ_n), as well as the gain (δ_g).

- The available power gain (G_a) or the operating power gain (G_w) specified can only be extracted as actual gain if the output impedance (G_a) or input impedance (G_w) of the transistor is conjugately matched to the load (G_a) or source (G_w). Assuming that this will (and can) be done, an output VSWR (G_a) or input VSWR (G_w) of unity is, therefore, expected after matching. Any tolerance in the controlling admittance presented to the input terminals (G_a) or output terminals (G_w) of the (modified) transistor will degrade this match. The worst-case deviation in the expected VSWR (δ_{vs}) is calculated and listed with the other sensitivity factors. The tolerance circle used for the gain or noise figure sensitivity factor is also used for the VSWR sensitivity factor.

A data file for the equivalent passive impedance-matching problem to be solved is created automatically after the option to modify the default name supplied for it has been used. The Impedance-Matching Module can then be launched to synthesize solutions to the defined matching problem. Note that the problem is solved in terms of the equivalent passive problem. The option to optimize the networks synthesized in terms of the active performance is provided in the results section of the Impedance-Matching Module.

7. ARTWORK GENERATION

As described above, the basic artwork for an ADW circuit is generated automatically from the electrical circuit description. Extensive graphical manipulation of the microstrip artwork is possible. This includes the following:

- Flipping stubs around.
- Adjusting the gap spacing or offsets vector used for a lumped component.
- Adjusting the dimensions of a line.
- Bending a line (optimum miter).
- Curving a line.
- Meandering a line.
- Tapering a step junction.
- Closing any misaligned voltage-shunt feedback loop or series block loop (two cascade networks connected in parallel) automatically. A suitable component must be selected before the loop is closed.

When a line is bent or curved or meandered, the physical length of the line is adjusted to keep the electrical line length unchanged. Note that physical line lengths may also be adjusted to compensate for step junction, T-junction or cross junction discontinuity effects. The adjustments are made to get the performance of the microstrip circuit as close as possible to that of the electrical circuit.

With the exception of nodal blocks and some components, ADW circuits can be exported to Microwave Office™. The script created by the ADW can be executed in Microwave Office to create the schematic of the circuit, as well as the associated artwork. Any residual discontinuity effects can then be removed by optimization before the circuit is manufactured. Any elements not available in the ADW can also be added at this stage.

Sonnet Software® files, as well as DXF or HPGL files can also be created for the ADW microstrip artwork. The Sonnet files and the DXF artwork can be used to verify or optimize the performance of the different microstrip networks designed in the ADW, or can be used to create simulation data for fitting models to passive components like single-layer capacitors, bond wires, spiral inductors and solenoidal coils.

It is a good idea to export individual networks for simulation in Sonnet's EM. Adjustments can be made to correct for discrepancies as the design proceeds and if the discrepancy is severe, a different network should be considered.

8. OPTIMIZATION AND OPTIMIZATION BY RE-SYNTHESIS

One of the final steps in an ADW design cycle is usually to optimize the completed design in the Analysis Module. (Note that, after the optimization, it is important to use the loop gain analysis feature to check the stability of each stage in the amplifier before the design is exported for further processing with another tool.) An Optimization Wizard is provided to set up the parameters of the error function to be used. Extensive control over the gain, the noise figure, the VSWRs, the stability factors (k, SSF and LSF), the maximum linear output power, the maximum linear power provided by each driver stage, and the maximum gain compression is provided. Error factors are also provided to prevent clipping of the intrinsic output voltage or current of a transistor on any of the four I/V-plane boundary lines allowed. It is also possible to control the amplification of the harmonics relative to the associated fundamental tone in wideband amplifiers. This is important in wideband amplifiers when low harmonic distortion is required.

The topology will usually not be changed when a circuit is optimized directly. The Synthesis Wizards can, however, be used to re-synthesize any of the any of the matching or modification networks in the amplifier. Note that the Two-port Command on the Schematic Toolbar can be used to replace any of the transistors used in the circuit with a different transistor, or the same transistor used at a different DC operating point, if necessary.

The wizards provided in the ADW are listed below, with a description of the function of each wizard.

General Impedance-Matching Wizard

The IIM, RMT, LMT and NOI commands can be activated by using this wizard. The different commands are described below:

IIM

This command can be used to set up an interstage impedance-matching problem. It can also be used to set up the matching problem associated with improving the input or the output match of the circuit.

The transducer power gain for the matching problem is set up automatically to level the overall transducer power gain of the circuit over the passband of interest. If a good match is required, the gain should be set to unity at each of the passband frequencies. This can be done in the impedance-matching section.

The source terminations for the left-hand side section of the circuit (section on the input side of the insertion point) are taken to be the actual source terminations of the circuit (as defined in the terminations block of the circuit file), while the load terminations for the right-hand side section are taken to be the actual load terminations.

RMT

The RMT command can also be used to set up an interstage impedance-matching problem, but instead of using the actual load terminations as load terminations for the section to the right of the insertion point (the output section), the terminations associated with the MAG (maximum available gain) of that section is used.

LMT

The LMT command is similar to the RMT command, but the input side of the section to the left of the insertion point (the input section) is terminated in its MAG terminations.

NOI

The NOI command is used to minimize the noise figure of the circuit section to the right of the insertion point (the output section). The circuit is assumed to be terminated on both sides as specified in the circuit file.

IVI Wizard

This wizard is used to set up an interstage impedance-matching problem to improve the input VSWR of the section to the left of the insertion point (input section) by mismatching its output impedance to the input impedance of the section to the right of the insertion point (output section). It can be used to improve the input VSWR of a low-noise amplifier. The gain of the amplifier can usually be leveled at the same time.

OVI Wizard

This wizard is similar to the IVI Wizard and is used to set up an interstage impedance-matching problem to improve the output VSWR of the section to the right of the insertion point (the output section) by mismatching its input impedance to the output impedance of the section to the left (the input section). As in the IVI case, the gain of the amplifier can usually be leveled at the same time.

CIL Wizard

This wizard is used to (re-)design an interstage or a load network to control the maximum linear output power (P_{out}), or the operating power gain (G_w) or the transducer power gain (G_T) of the section to the left (on the input side) of the insertion point. Note that information on the detailed performance (efficiency, gain, power, noise figure, stability factors, etc.) at each point on the contour is provided. If necessary, a point match can be enforced.

CIR Wizard

This wizard is used to (re-)design an interstage or a source network to control the noise figure (F), or the available power gain (G_a) or the transducer power gain (G_T) of the section to the right (on the output side) of the insertion point. Information on the detailed performance (efficiency, gain, power, noise figure, stability factors, etc.) at each point on the contour is provided. If necessary, a point match can be enforced.

MOT Wizard

This wizard is used to (re-)synthesize the modification network of a transistor and/or to replace the current transistor in an amplifier chain. It sets up the information required by the Device-Modification Module to insert a new stage (a transistor with its modification networks) at the insertion point.

9. REFERENCES

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