

OVERVIEW OF DESIGNING THE LOAD MATCHING NETWORK FOR A POWER AMPLIFIER BY USING THE CIL WIZARD PROVIDED IN THE AMPSA ADW

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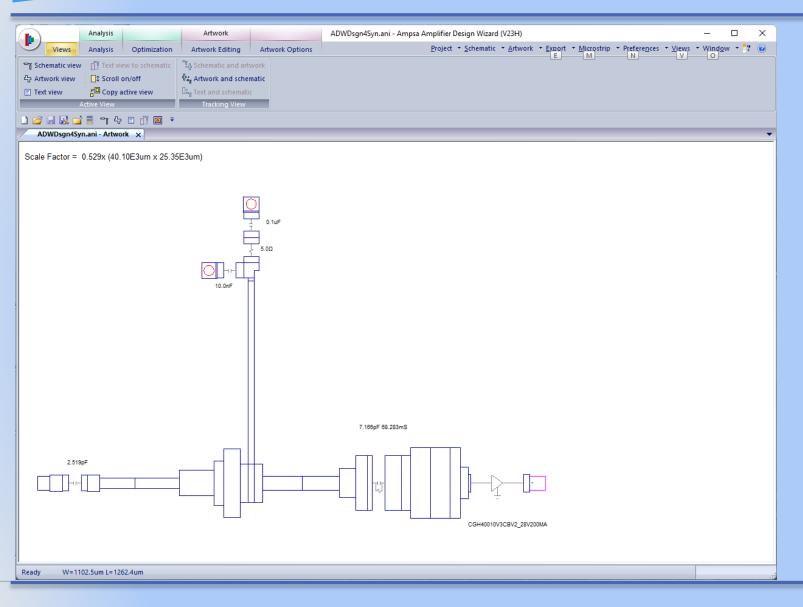
The ADW is setup to design single-ended amplifiers. Note that Doherty amplifiers, balanced amplifiers, push-pull amplifiers, amplifiers with symmetrical combination networks and even some load modulated balanced amplifiers can all be converted to equivalent single-ended stages.

The Ampsa ADW CIL wizard can be used to set up a large variety of matching problems for an amplifier stage. Different classes of operation can be targeted. These include continuous modes of operation.

In this presentation, the CIL wizard will be used to setup the specifications for the load matching network of a 1.0 - 3.9 GHz 10W amplifier. Solutions to the defined problem will also be synthesized by using the impedance-matching wizard provided in the ADW.

The Macom CGH40010F GaN transistor will be used in this example. An ADW model was fitted to the transistor biased at 28V 200mA (Class-AB operation). Class-B operation will be targeted in this presentation, but the same design flow can be used for other classes of operation.

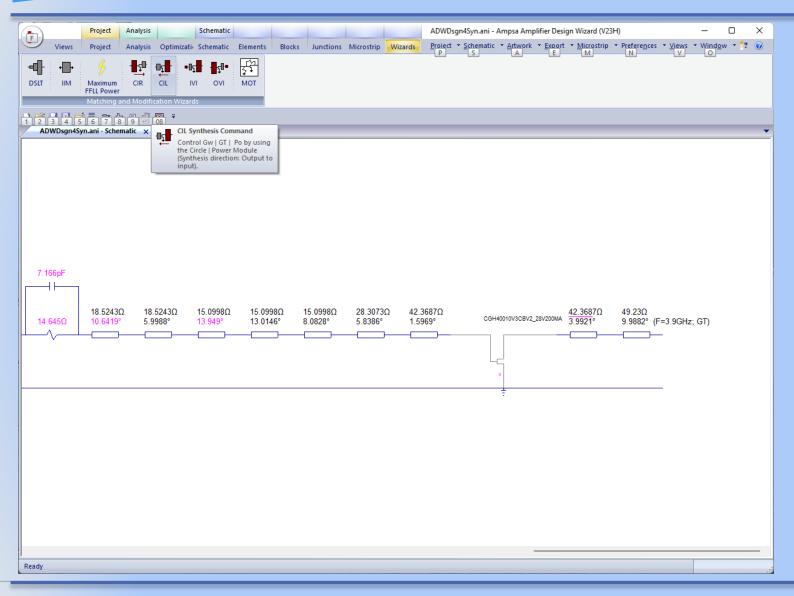




The circuit shown will be used as a starting point for the design. The input matching network is from a previous design, but the design flow is still valid without an input matching network in place. (Stabilizing the transistor, at least inside the passband is, however, advisable.) The input network can be optimised when the load network is in place.

Note that the schematic or the artwork or the text description of the circuit can be viewed. Use the commands provided on the quick access toolbar (QAT) to switch between views.

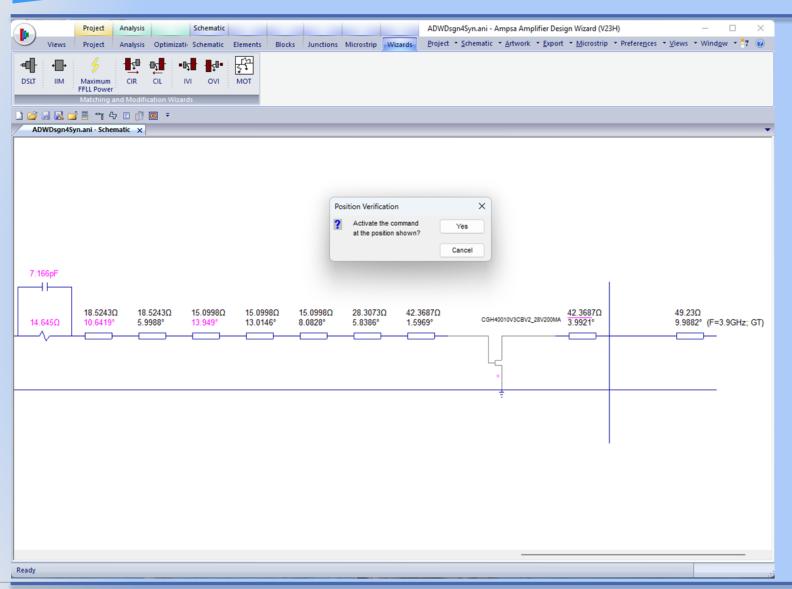




The ADW synthesis wizards must be launched with a schematic view active. The insertion point for the matching network required must be selected before launching the wizard.

Note that an element in the schematic is selected by left-clicking one of the labels associated with the schematic element. In an artwork view, the artwork element to be selected is left-clicked.



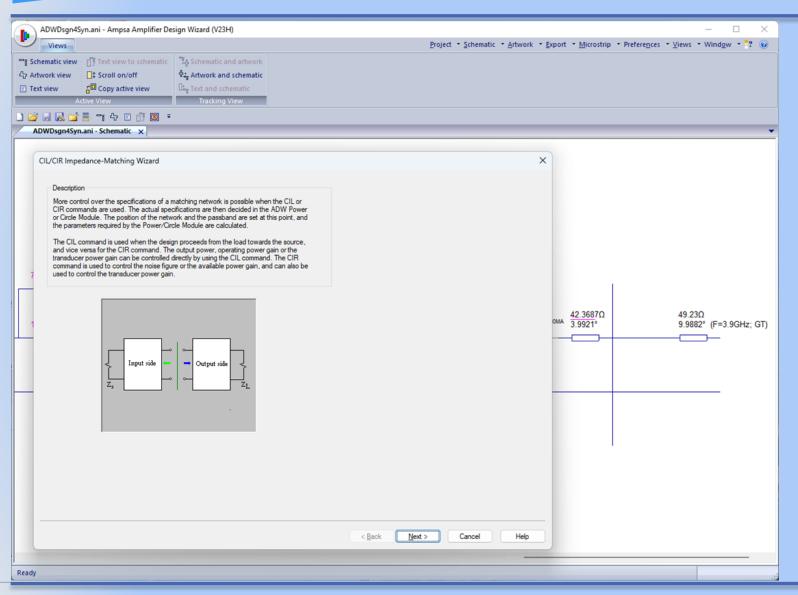


The CIL wizard was launched by selecting the Schematic | Wizards | CIL ribbon command.

The schematic will be split as shown by the command.

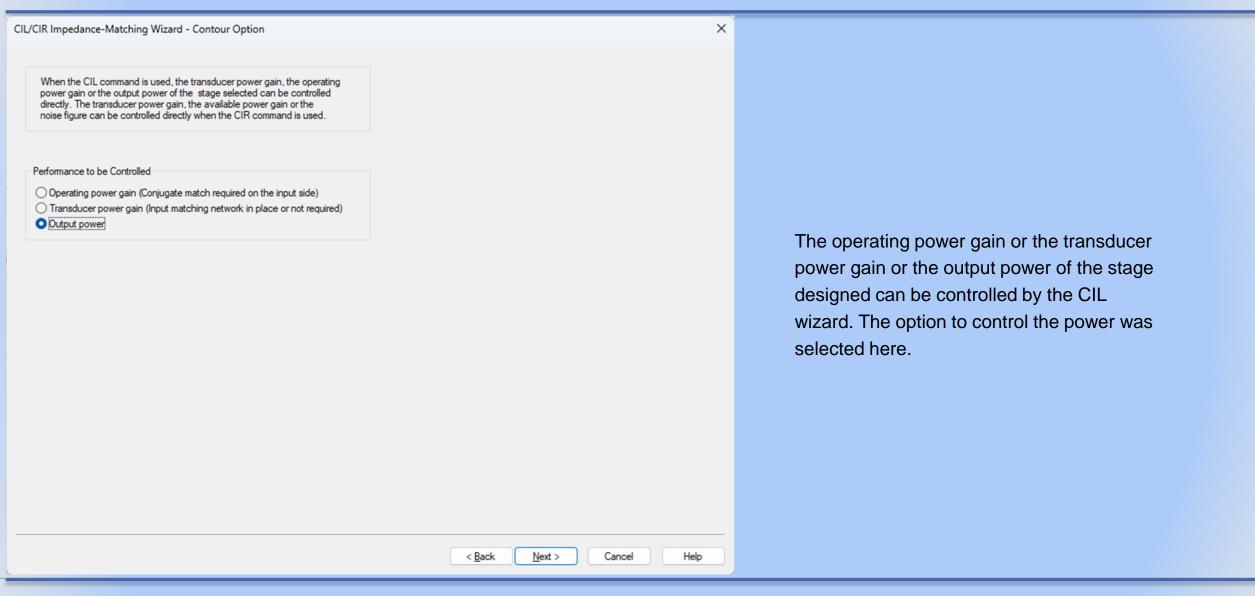
The matching network to be designed with the CIL wizard can be the load network for the output stage or any driver stage in the amplifier. A multistage power amplifier is designed by starting with the load network.



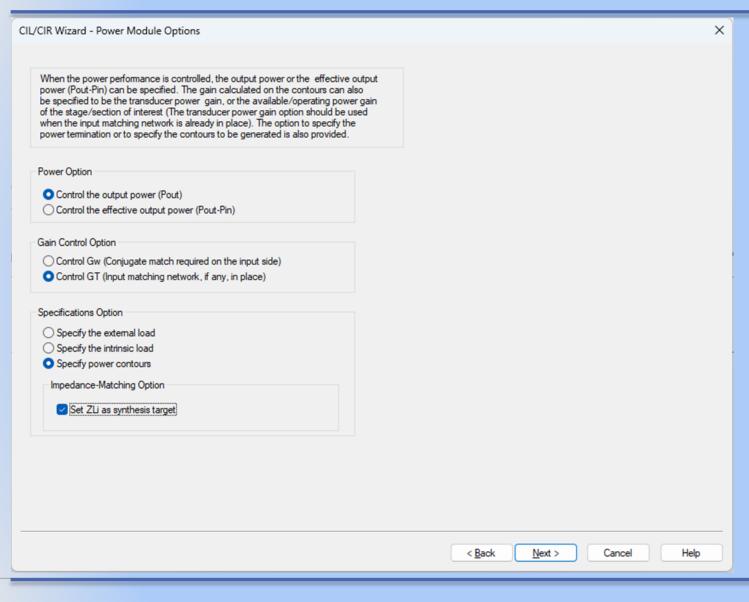


The first page of the CIL wizard is displayed here.









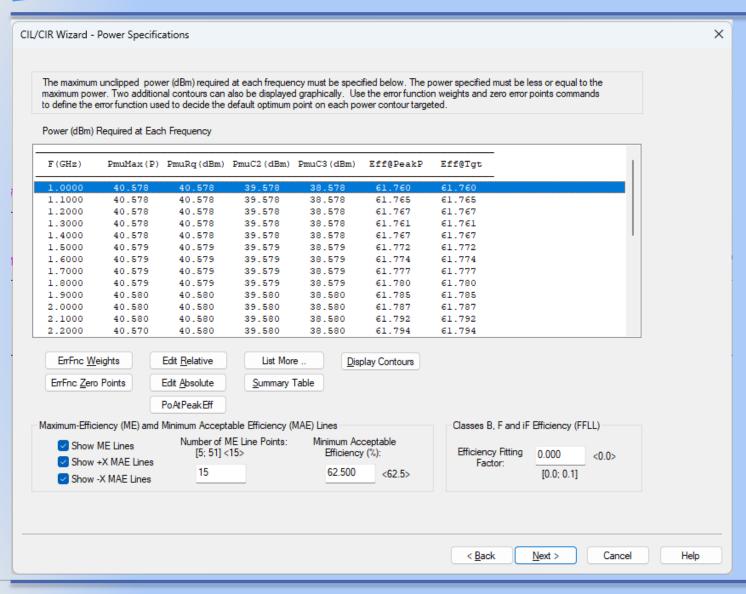
The output power or the effective output power can be controlled. Use the effective output power when the transistor gain is low or when a matching network for an oscillator is designed.

When an input matching network is already in place, the gain to be controlled is the transducer power gain. This option was selected here.

The power contours option was selected here. The alternatives are to control the intrinsic or external load terminations directly.

Note the option to use the intrinsic load terminations as synthesis targets. When this option is not selected, the input terminations presented by the matching network at the insertion point are used as targets.





The power levels of interest must be specified on this page. Constant power contours can also be generated at two additional power levels at each frequency.

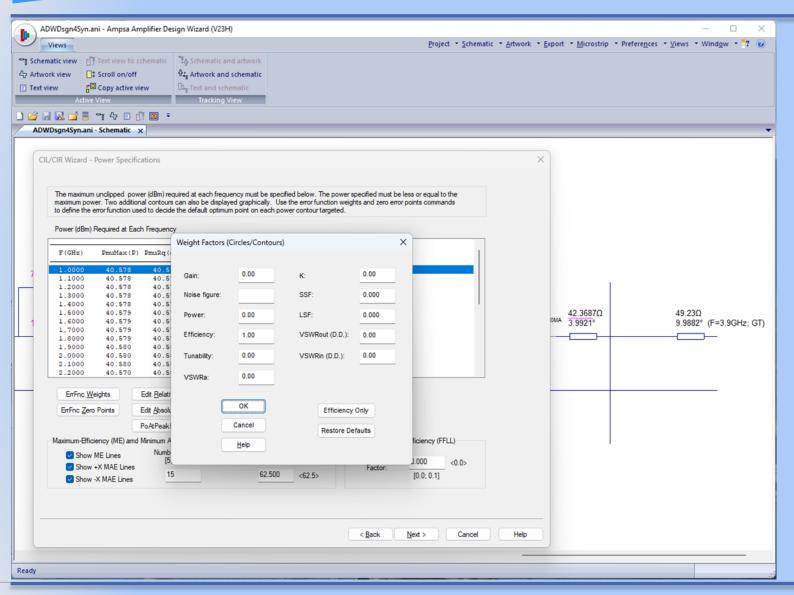
The error function used to select the optimum point on each contour is set by using the Error Function Weights and Zero Error Points commands.

Edit Relative or Edit Absolute are used to set the contour power levels.

The efficiency associated with the peak power points and the maximum efficiency associated with the contours targeted are also listed in the table.

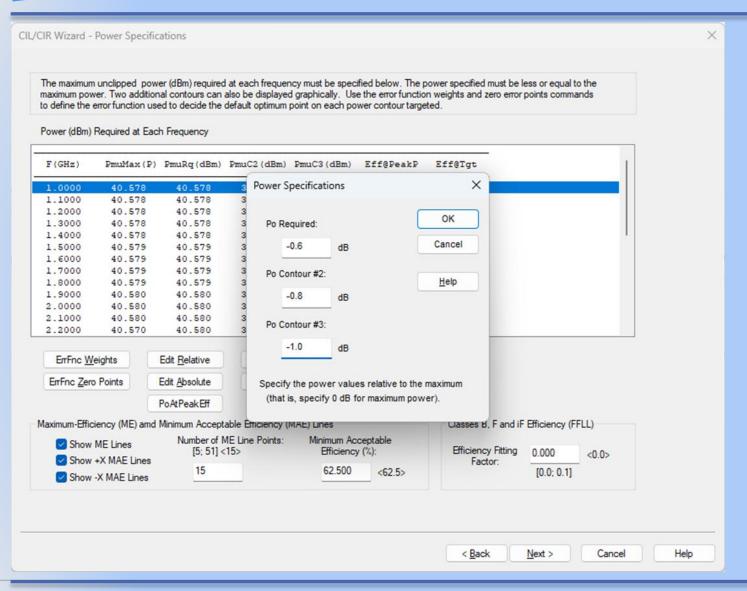
Note that the minimum acceptable efficiency must be specified for the efficiency lines to be displayed. (With the exception of a Class-A stage, the efficiency will vary on the circumference of each power contour.)





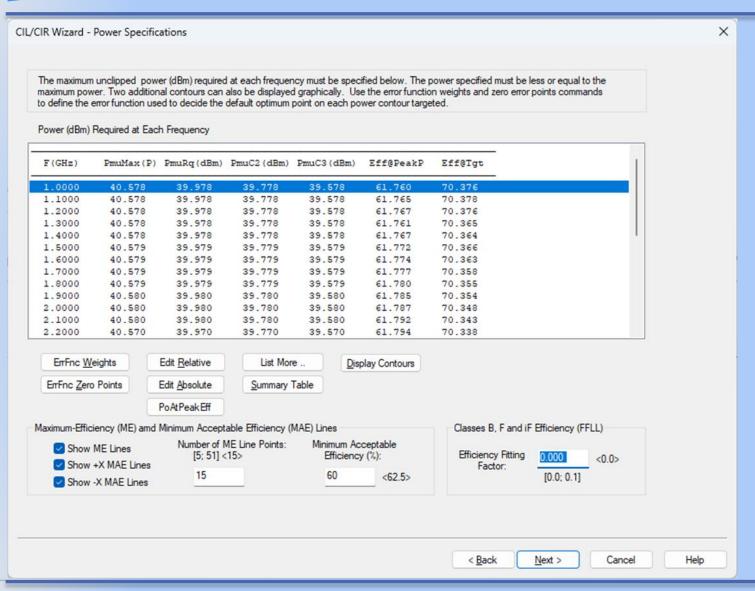
The option to use only the efficiency to decide the optimum point on each constant power contour targeted has been selected (Error Function Weights command).





The Edit Relative command has been selected to set the power levels for the contours to be generated. The power level targeted is 0.6 dBm below the peak power.





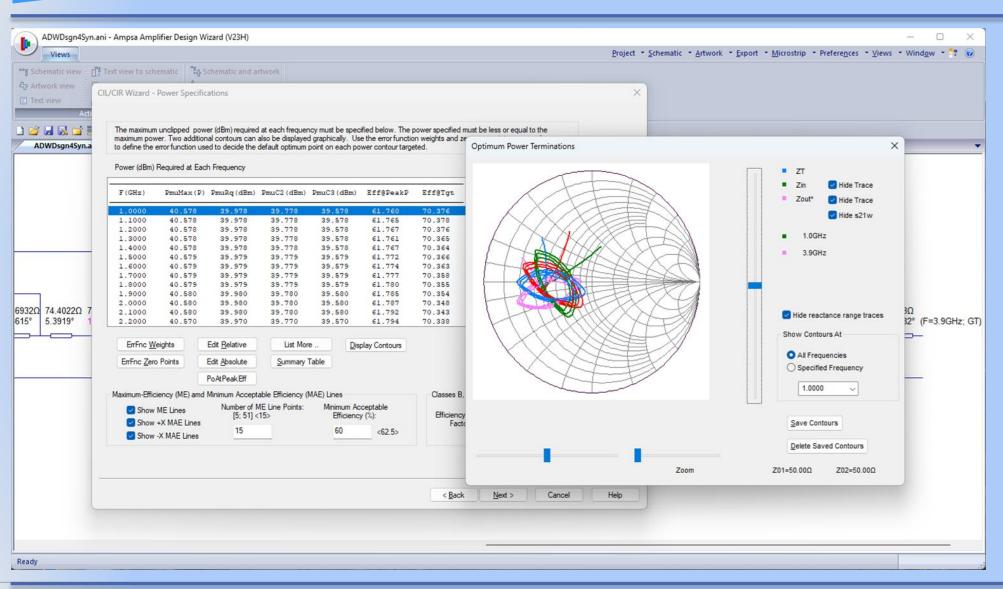
The power listed here is the maximum unclipped output power (P_{mu}).

Efficiencies (drain efficiency) above 60% are targeted.

The List More command can be used to list the peak efficiency obtainable at different power levels.

The Display Contours command can be used to display the constant power contours and the maximum efficiency lines.



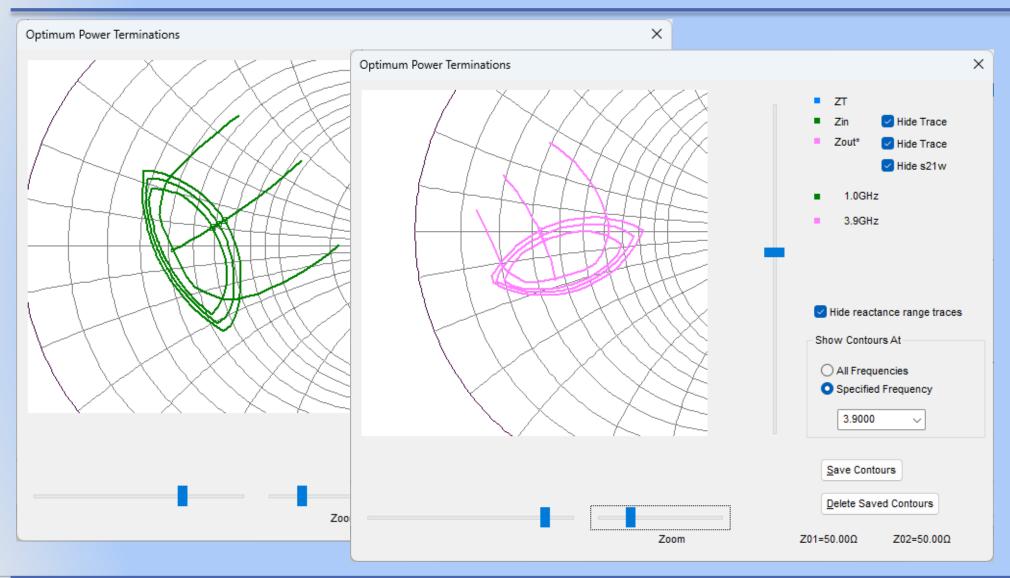


The constant power contours targeted are shown here with the maximum efficiency lines.

The intrinsic load impedance is purely resistive at the maximum efficiency point on a power contour. This point is located on the voltage clipping side of the power contour.

Note the anti-clockwise rotation of the maximum efficiency lines with increasing frequency (green to magenta). Also note the area in which all the constant power contours intersect and the area in which the maximum efficiency lines intersect.



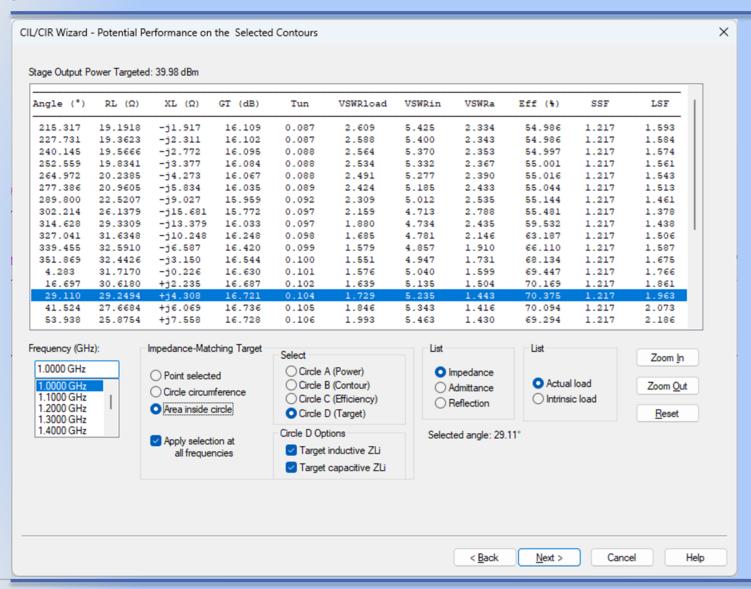


The constant power contours and the efficiency lines at 1.0 GHz and 3.9 GHz are displayed here.

Three efficiency lines are shown with the power contours at each frequency. The two lines away from the maximum efficiency line are constant efficiency lines.

Efficiencies above the targeted level can only be obtained on the contour sections defined by the two constant efficiency lines.



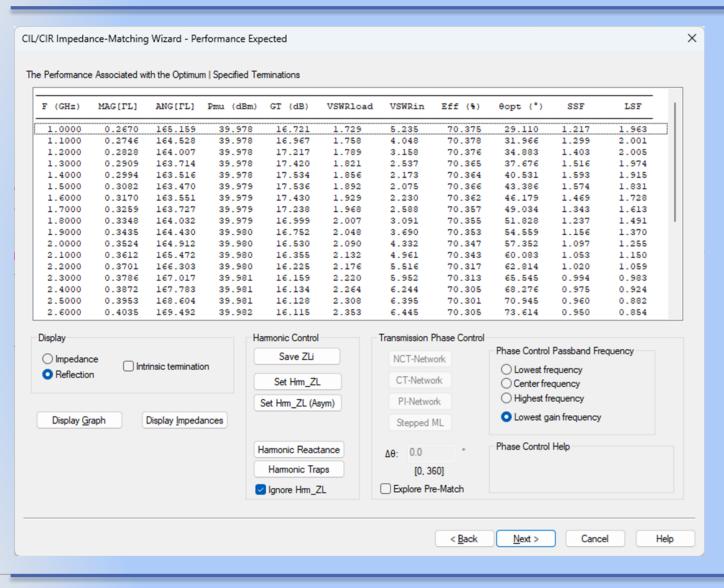


The performance on the circumference of a constant power contour is listed here (select the frequency of interest from the list provided). The optimum point selected on the contour is high-lighted and can be changed.

A circle (fundamental frequency targets) can be fitted automatically to each contour or the optimum point on each contour for impedance-matching purposes.

The option to target circles centred on the optimum point of each contours was selected here. The area inside each of these circles will be targeted.





The performance at the optimum point on each power contour is listed on this page.

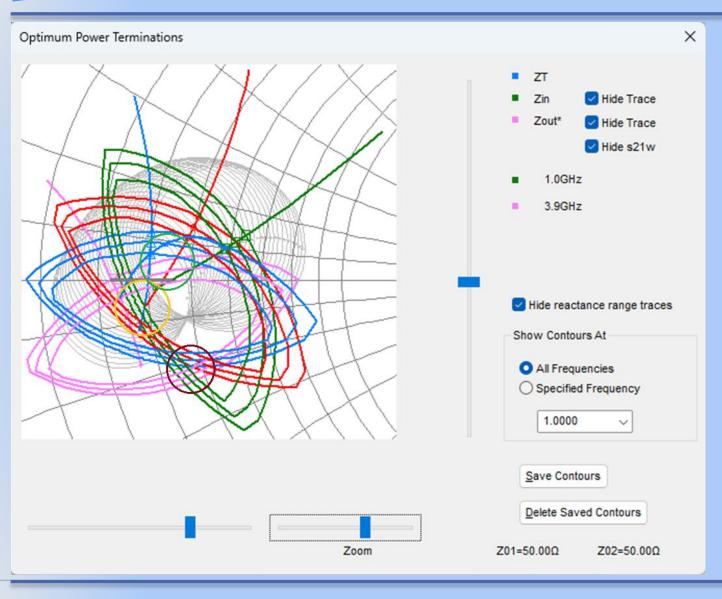
The Set Harmonic ZL and Set Harmonic ZL (Asymmetrical) commands can be used to set impedance-matching targets for the harmonic terminations. Class-B operation will be targeted here.

Note the Harmonic Traps command. Harmonic traps can be added to the matching networks to be synthesized as fixed elements by using this command. The option to export the traps selected directly to the circuit file is also provided.

The Explore Pre-Match option (CMA networks) provides an alternative to the Impedance-Matching module. The transmission phase-shift can be controlled directly by using this option (The CMA networks are derived from PI-networks and T-networks; two cascaded lines are also allowed). The intrinsic load terminations cannot yet be controlled directly by using this option.

The pre-match option will not be used in the presentation.





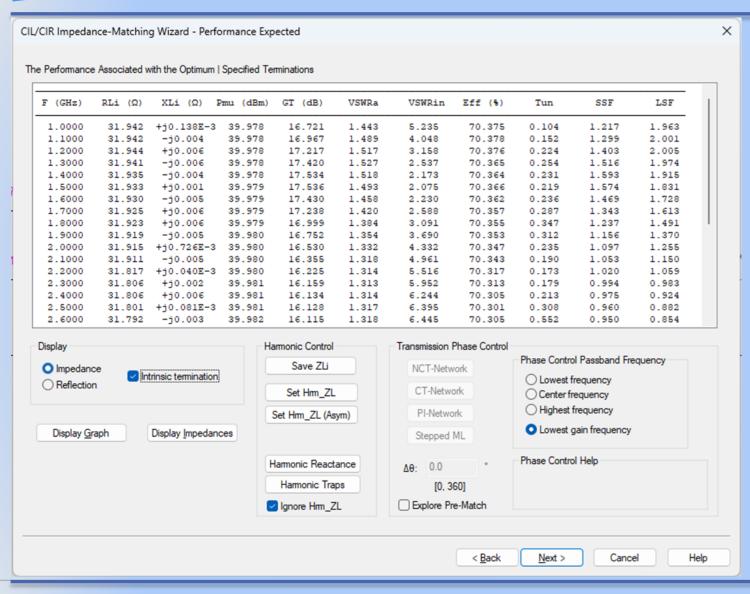
The Display Graph command provided on the wizard page was used to display the circles to be targeted in the Impedance-matching module. The constant power contours and the maximum efficiency lines are also shown.

Note that the origins of the maximum efficiency lines are located in a relatively small area. This area can be targeted by targeting power levels close to the peak levels. A good alternative is to target the line segment defined by the intersects of the maximum efficiency lines with the zero reactance line. This can be done by using a segmented taper transmission line.

Also note the eye formed by the circles targeted here. This area could also be targeted.

Power close to the targeted levels can be obtained at all of the frequencies shown by targeting the red circle at the bottom of the plot. The efficiency will, however, be lower that the level targeted.

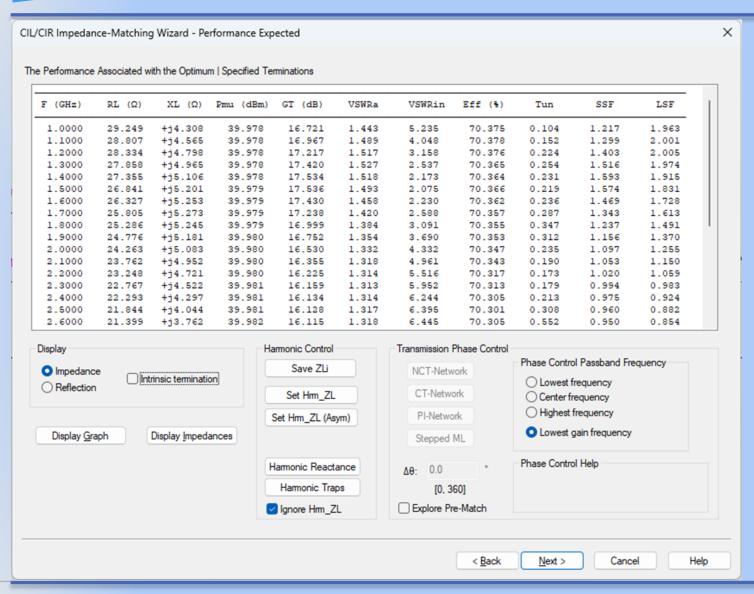




The performance at the optimum point on each power contour is listed in the table shown.

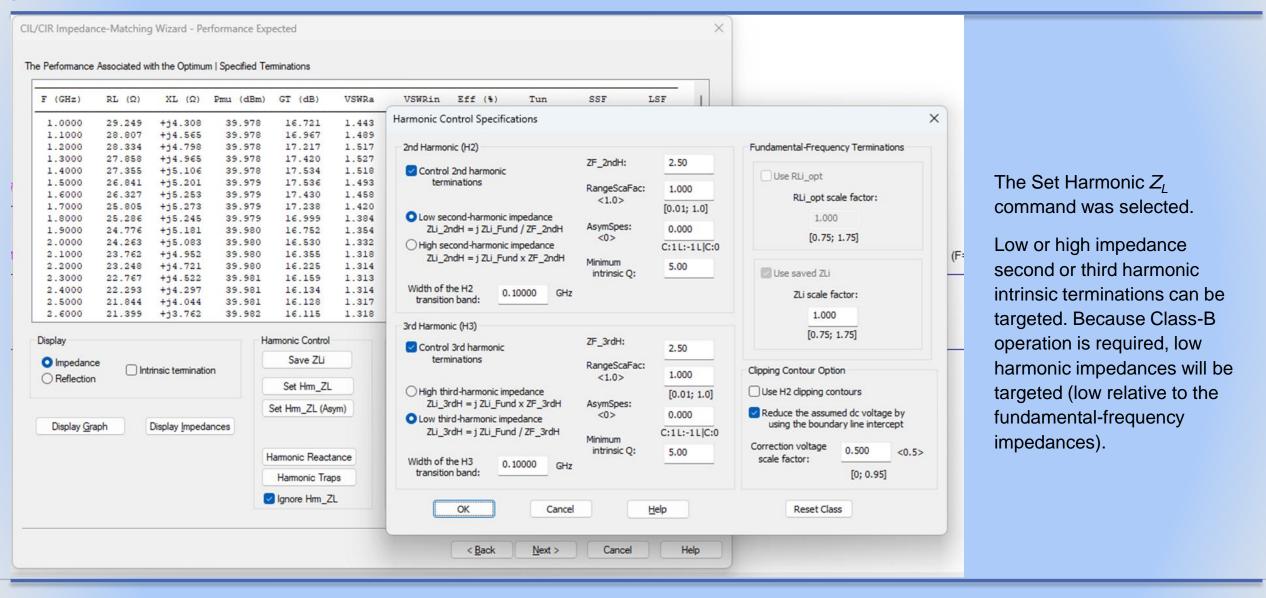
The intrinsic load impedance targeted is around 31.9 Ohm. The impedance required at the insertion point for the matching network is around 29 Ohm and lower (see the next slide). Take note of these levels. When the matching networks synthesized do not allow for biasing the transistor, fixed components can be added to the matching network. Any extra shunt elements added should ideally present impedances significantly higher than the impedances targeted (say, at least three to four times higher).



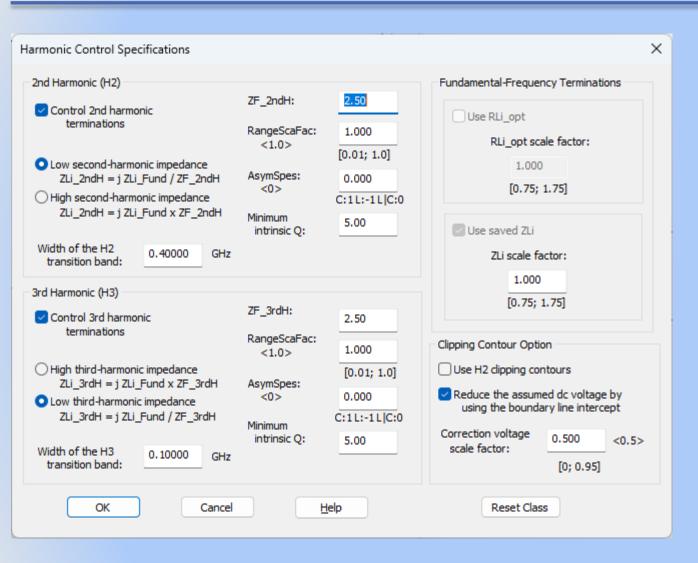


The impedance required at the insertion point for the matching network is around 29 Ohm and lower.





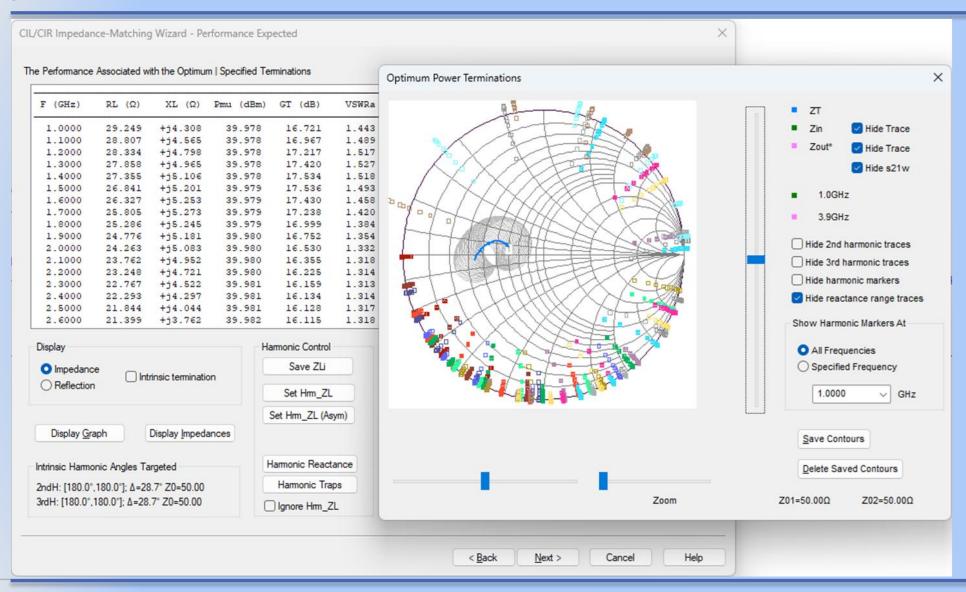




The second and third harmonic bands in this example overlap the passband. The third harmonic band also overlaps the second harmonic band. The fundamental targets override the harmonic targets in the ADW, while the second harmonic targets generally override the third harmonic targets.

Transition bands can be defined for the second harmonics and the third harmonics. 0.4 GHz will be used for the second harmonic and 0.1 GHz will be used for the third. Because shorts are required for both harmonic bands, the transition band for the third harmonic could be set to zero.

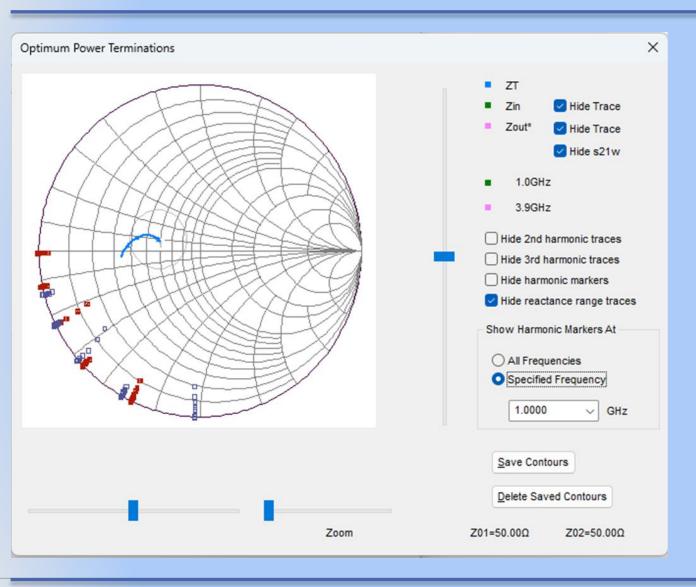




The fundamental-frequency and harmonic targets at the insertion point for the matching network.

Options are provided to hide the third or the second harmonic targets.



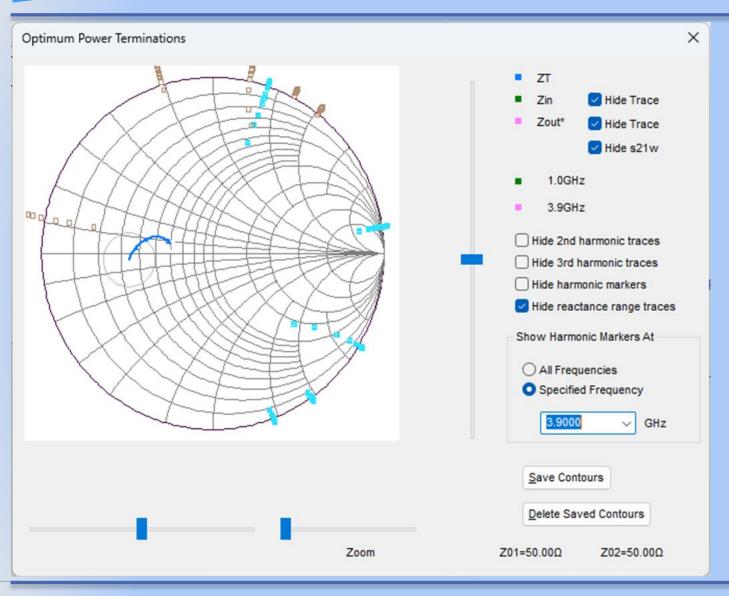


The targets can be displayed for all the passband frequencies or for a specific passband frequency. The associated intrinsic impedances will be near shorts for terminations at the centre of the range of external reflection coefficients shown for each harmonic.

Harmonic sectors are fitted automatically to the areas defined by the harmonic markers. A sector is defined by a local origin and two intersects with the Smith chart edge.

Harmonic sectors will also be fitted to the intrinsic targets if the relevant option was selected.





The second and third harmonic targets associated with 3.9 GHz.

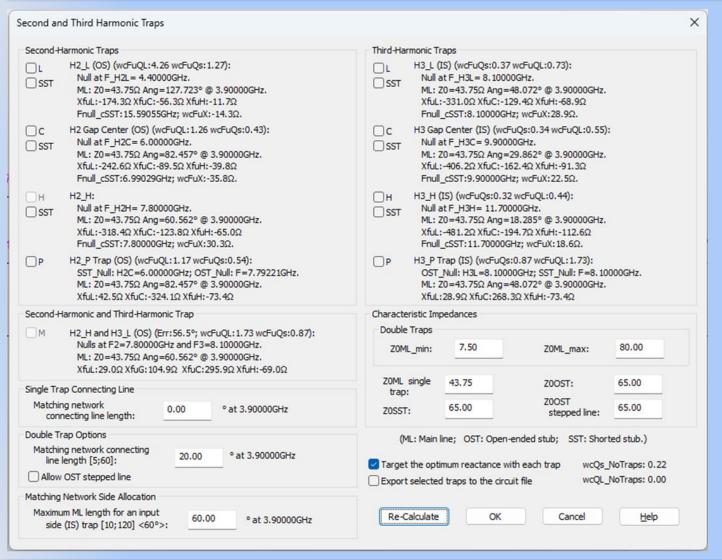
Note that the harmonic areas to be targeted rotate anti-clockwise with frequency. It will not be possible to obtain near shorts for all the harmonics with the passband targeted here.



fund (GHz)	XB_2ndH	XE_2ndH	XB_3rdH	XE_3rdH
1.0000	-31.717	-0.387	-48.367	-6.728
1.1000	-34.418	-1.636	-55.621	-8.714
1.2000	-37.377	-2.891	-64.655	-10.768
1.3000	-40.643	-4.154	-76.389	-12.911
1.4000	-44.277	-5.434	-92.242	-15.162
1.5000	-48.352	-6.730	-115.269	-17.546
1.6000	-53.020	-8.047	-152.095	-20.096
1.7000	-58.364	-9.394	-220.744	-22.849
1.8000	-64.599	-10.774	-397.504	-25.850
1.9000	-72.008	-12.191	-1.935E3	-29.156
2.0000	-80.969	-13.654	673.029	-32.846
2.1000	-92.114	-15.169	285.427	-37.018
2.2000	-105.710	-16.767	182.323	-41.846
2.3000	-124.279	-18.413	131.914	-47.440
2.4000	-150.320	-20.133	102.421	-54.095
2.5000	-189.165	-21.944	83.037	-62.204
List				ОК
Reflection coefficients (Z0=50)				Cancel
Reflection coefficients (Z0sc)				
Reactance values				Help

The reactance ranges to be targeted for the second and third harmonics are listed here. Note the anticlockwise rotation of the targets with increasing frequency.





Harmonic traps can be used to provide the required intrinsic impedance at specific frequencies. Potential traps are listed here for a number of second and third harmonic frequencies. When an SST option is set, the trap will be created with a shorted stub. The default is to use an open-ended stub.

When the series transmission line (ML) associated with a trap is short, the trap can be added to the circuit before a matching network is designed. Traps with longer main lines can be added on the output side of the matching network, but it is unlikely that the desired transmission phase shift required for an intrinsic short will be obtained with the matching network in place. The harmonic will, however, be filtered from the output.

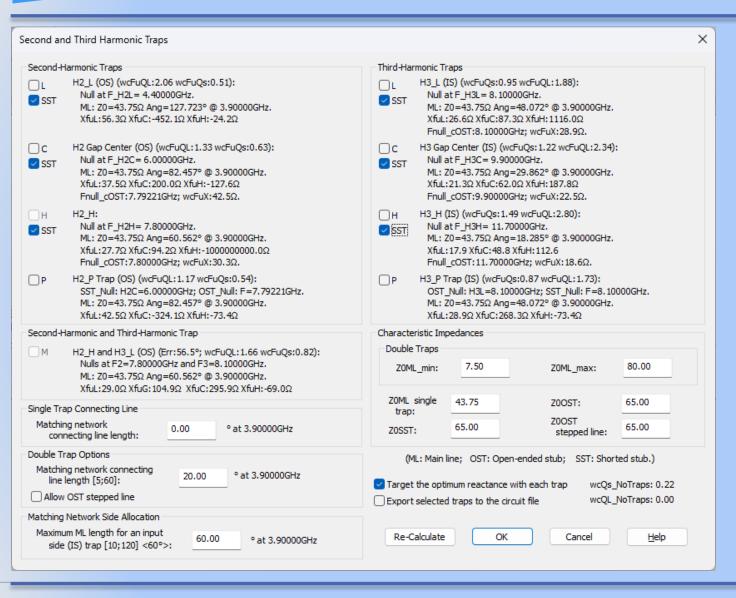
Note that the traps marked with a P consist of a shorted stub in parallel with an openended stub.

Ideally a trap should not load the circuit significantly at the fundamental frequencies. The loading imposed is measured by calculating the worst-case fundamental-frequency source and load Qs, as well as the shunt reactance presented by the trap at a number of passband frequencies. The worst-case Qs of the terminations (no loading) are listed in the lower RHS corner of the table.

The trap with the shortest main-line length (18.285 degrees at 3.9GHz) is the 11.7 GHz trap. The loading associated with this trap will be minimal. Note that the H2_P trap may be a good option for feeding in the drain bias. The shunt impedance presented is higher than 42.5 Ohm inside the passband (still significant).

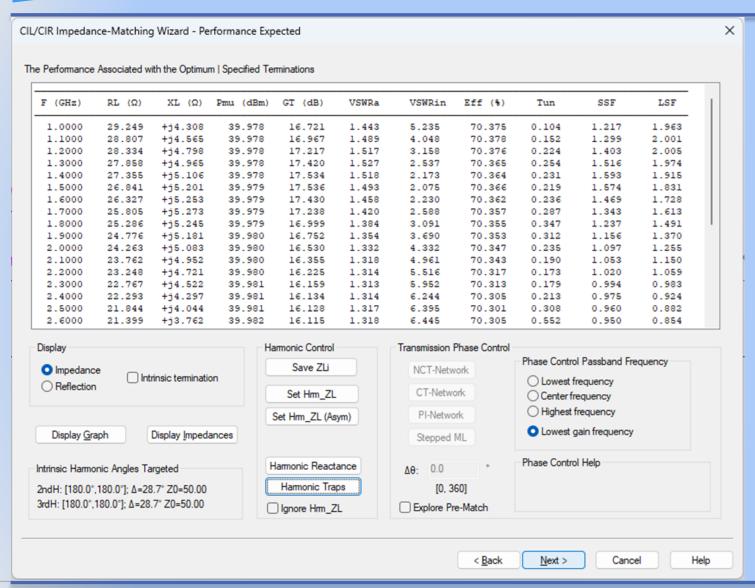
Up to two traps can be selected from the table. The selected traps can be exported directly to the circuit file or can be added as fixed components to the matching networks to be synthesized.





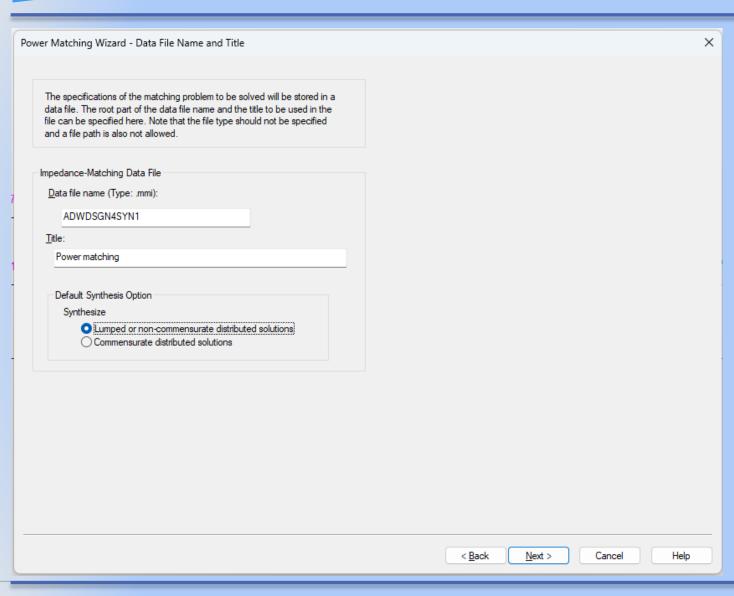
The SST options were set here to view the loading associated with shorted stub traps. The loading of the 6.0 GHz second harmonic trap is above 37.5 Ohm in the passband, but this is not high enough to not have a degrading effect on the performance.





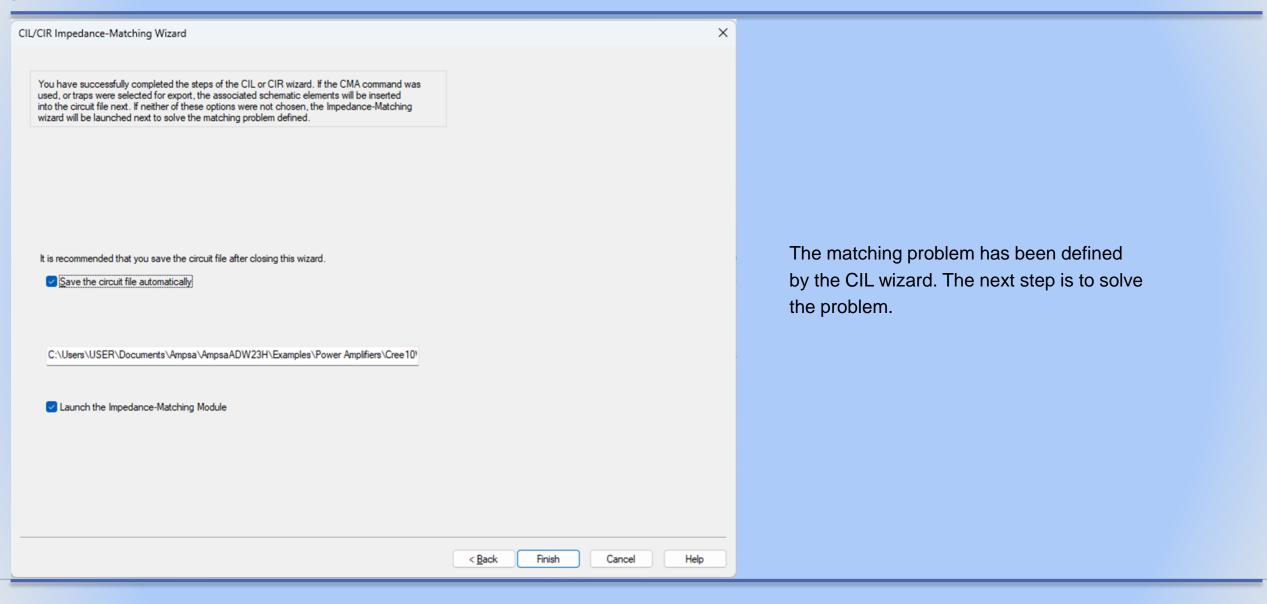
The Next command has been selected to proceed to solving the defined matching problem.



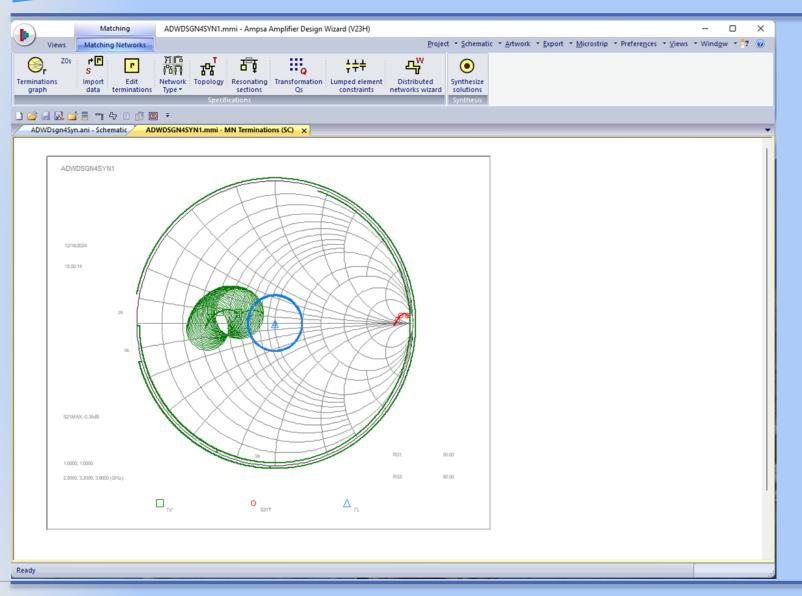


The default name for the matching network file is shown here. The option to solve the matching problem with non-commensurate networks was selected.





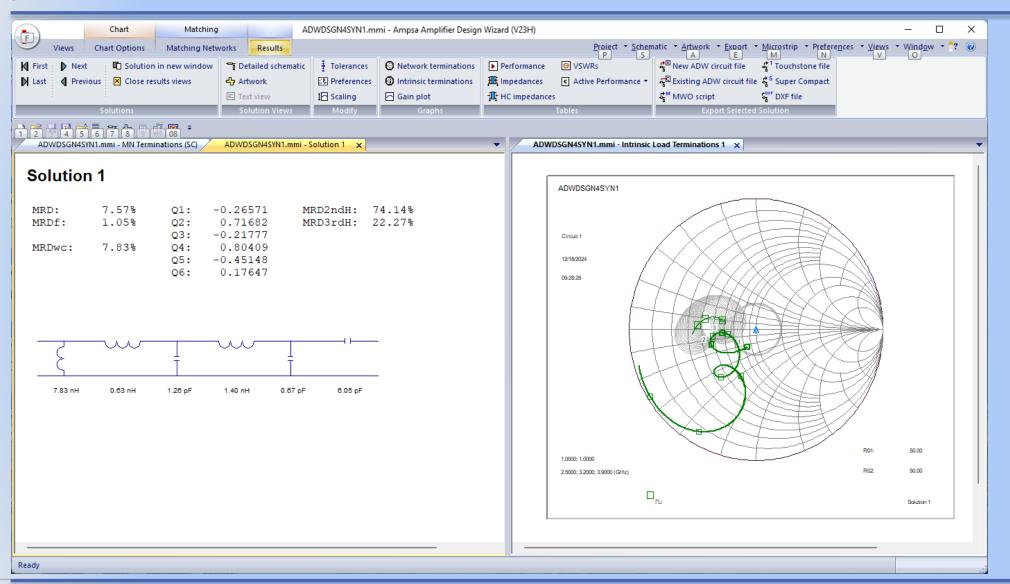




The Matching wizard was launched and impedance-matching networks can now be synthesized.

Solutions to the matching problem will be synthesized next.

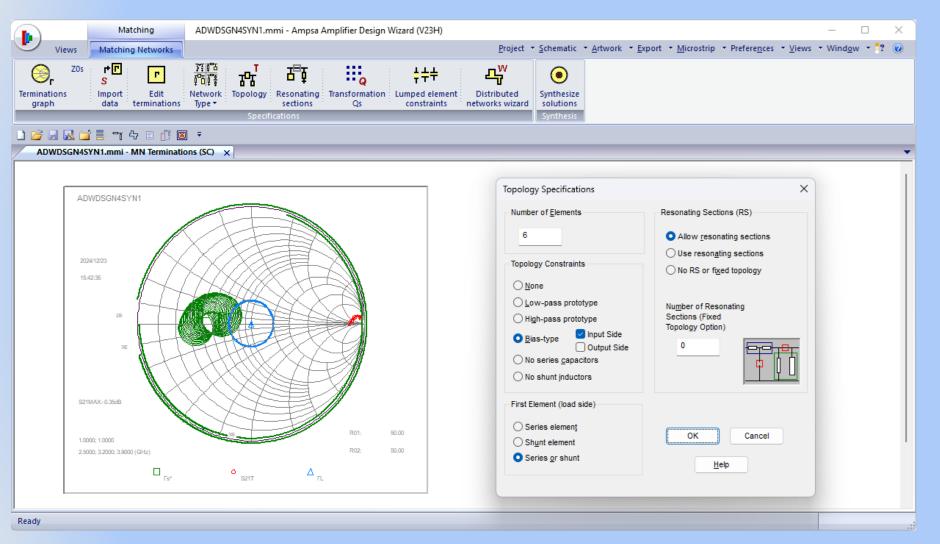




It is generally a good approach to try lumped solutions to a matching problem first (Use the Network Type ribbon command). Insight into the problem can be gained by doing this before proceeding to distributed solutions.

A lumped solution to the matching problem is shown here. The drain bias can be fed in through the inductor if the *dc* short is replaced with an RF short.



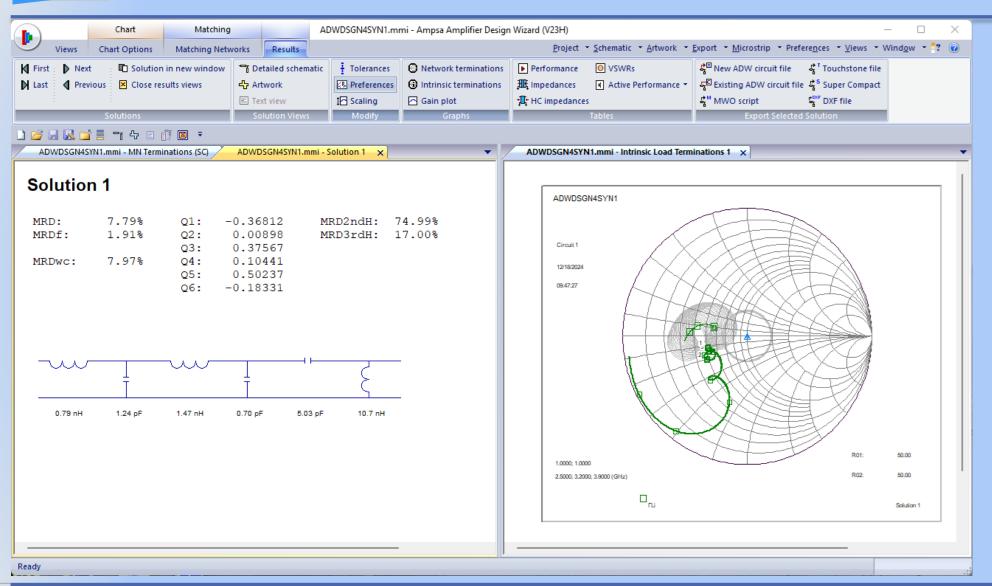


The topology constraints used when the lumped solution shown was synthesized.

Note the bias-type option.

Options are provided to synthesize networks allowing biasing on the input and/or output sides of the matching networks.

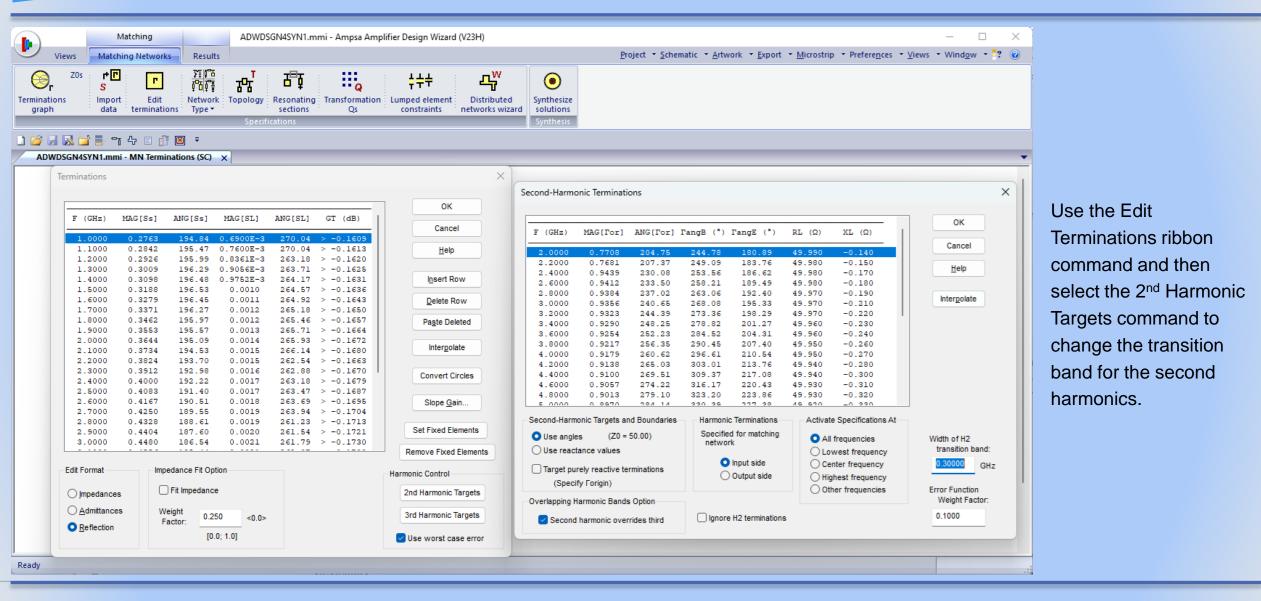




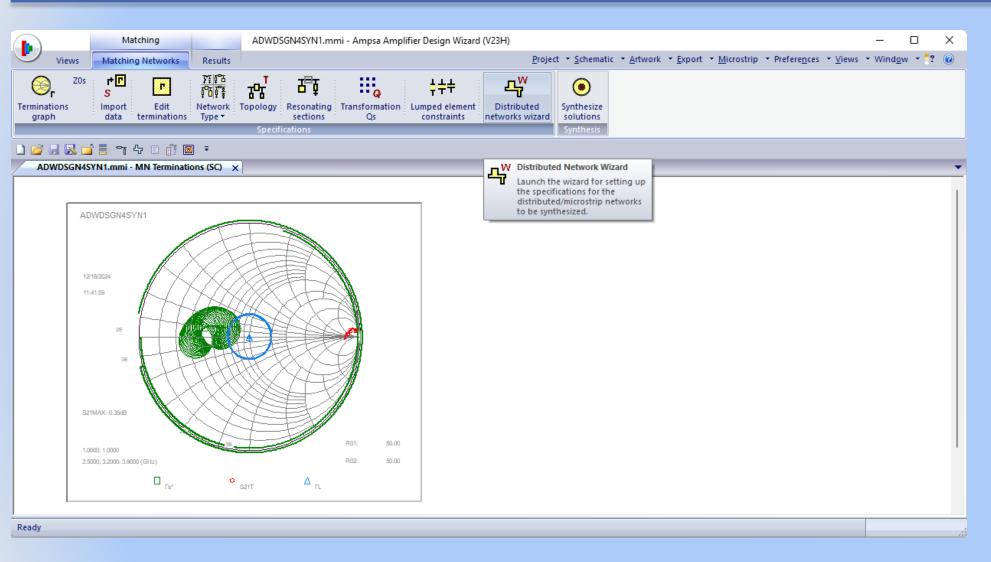
The effect of reducing the second harmonic transition band to 0.3 GHz is shown here.

A conical coil or a solenoidal coil can be used to feed in the drain bias.





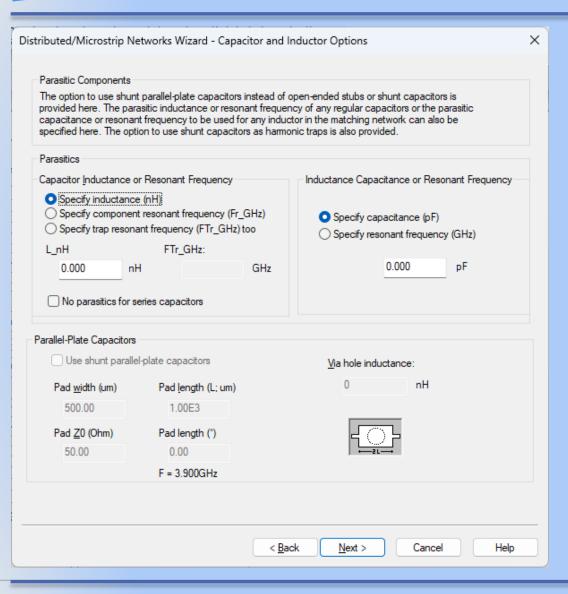




Distributed networks will be synthesized next.

The Distributed Networks
Wizard is used to change
the specifications for
distributed networks. Use
the ribbon command
shown to launch the
wizard. Any results views
must be closed before the
wizard can be launched.



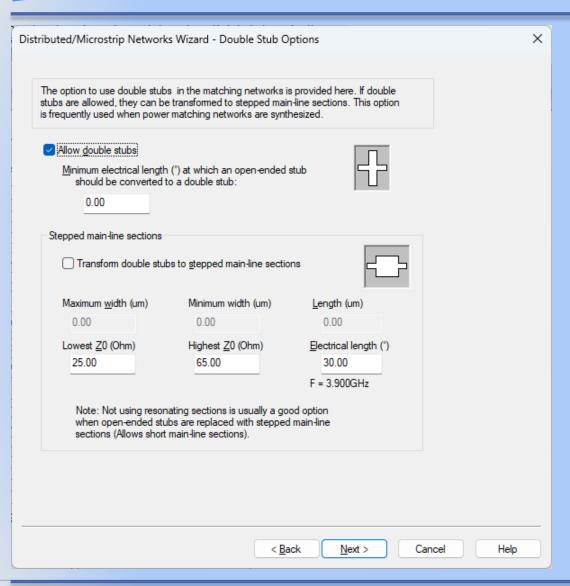


Parasitic inductance and capacitance can be specified for capacitors and inductors on this page.

The parasitic inductance or the resonant frequency for the capacitors can be specified. The option to use the shunt capacitors as harmonic traps is also provided.

Ideal lumped components will be used in this presentation.



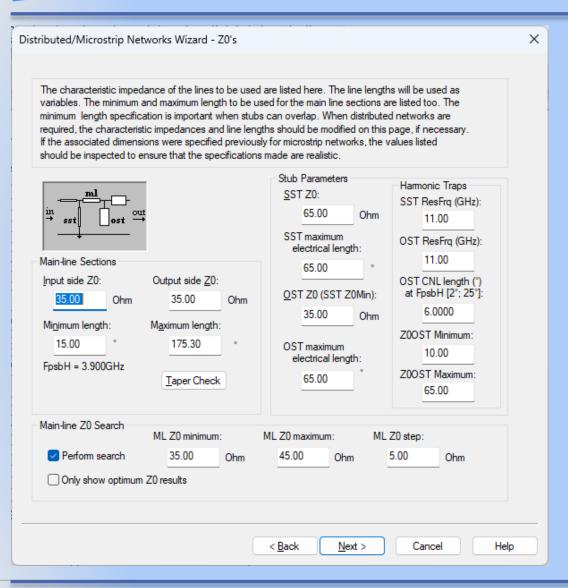


When it is possible, open-ended stubs in an ADW matching network can be transformed automatically to equivalent mainline sections.

A minimum electrical length can be set for the transformation.

The phase responses of the networks synthesized are generally better behaved when this is done.





When the characteristic impedance specified for a stub allows it, the stub can be designed to provide a transmission null at a specified frequency in addition to providing the fundamental-frequency reactance required.

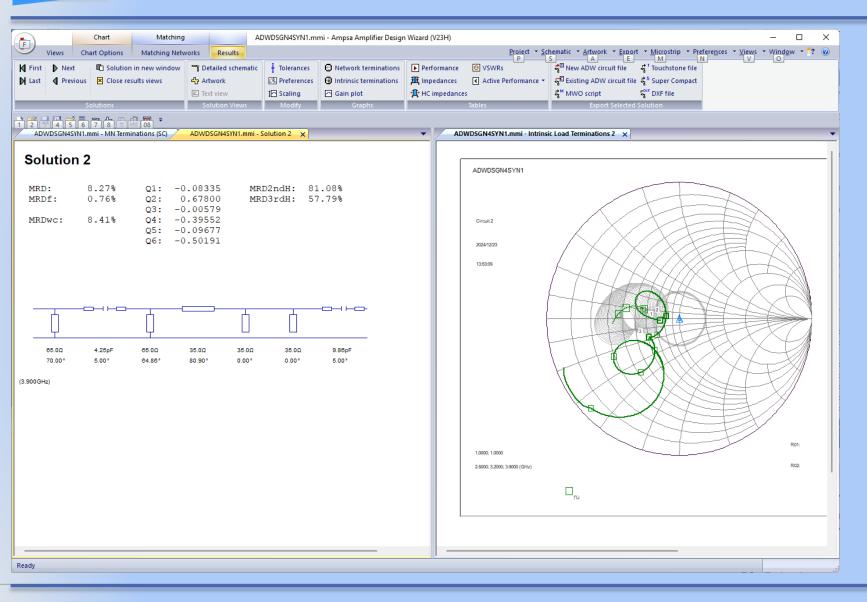
Different null frequencies can be set for the shorted stubs and the open-ended stubs.

If the option to transform the open-ended stubs to main-line sections was selected, the open-ended stubs will not be used to trap the harmonics.

Some experimentation with the trap frequencies is usually required. Start by setting the resonant frequencies to frequencies in the transition bands.

In this example, the transmission null frequencies were set to 11.0 GHz.

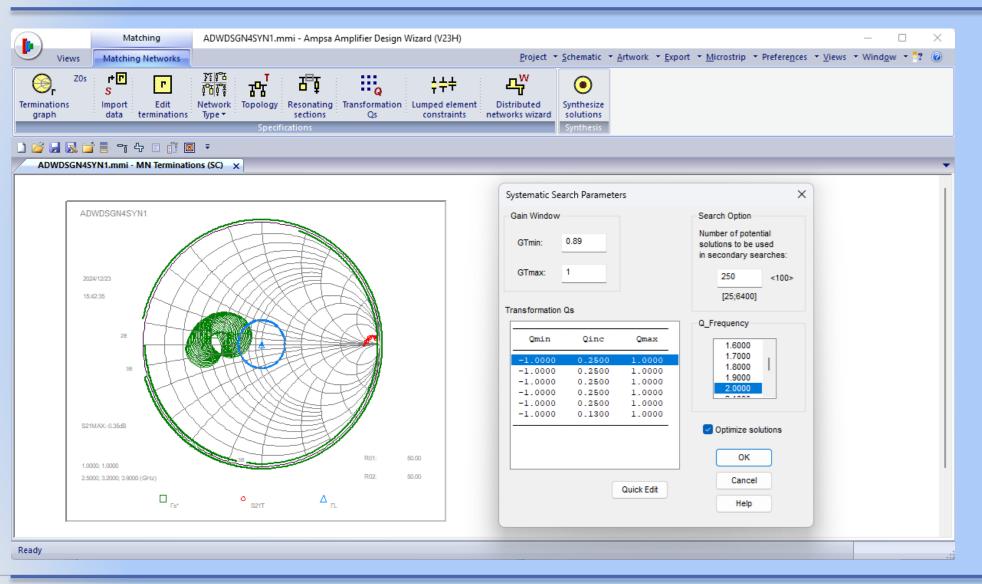




The second solution obtained with the specifications shown.

Note that the absolute values of the transformation-*Q* associated with this solution is small (less than 0.68). Better solutions may be obtained by scaling the range of the systematic search done down.



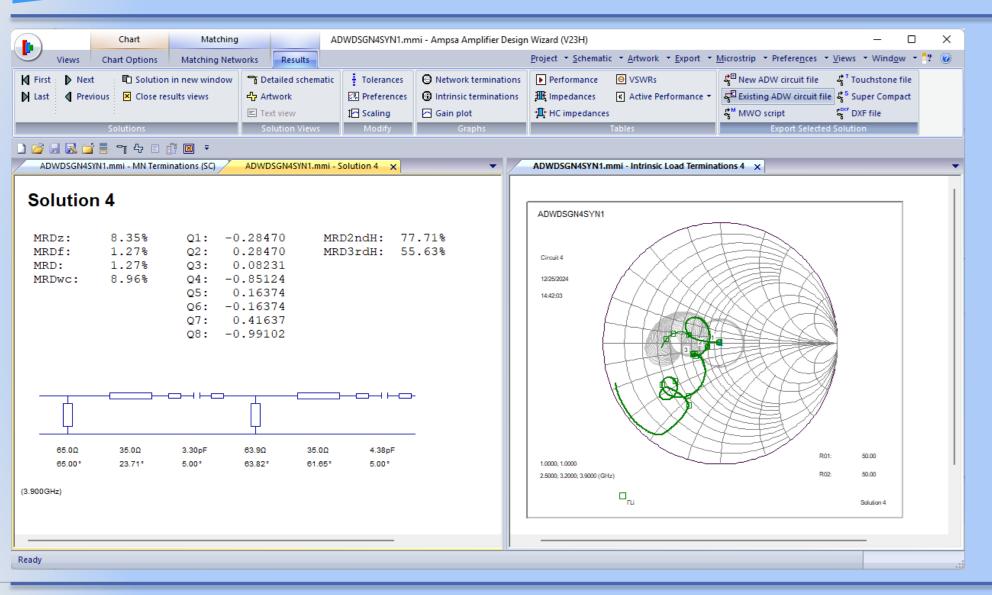


The range of the search was scaled down and the number of potential solutions to be used in secondary searches was increased.

The Transformation Qs ribbon command was used to open the dialog box shown.

To keep the run-time similar, the Q increment should be scaled by the same factor as the boundaries.

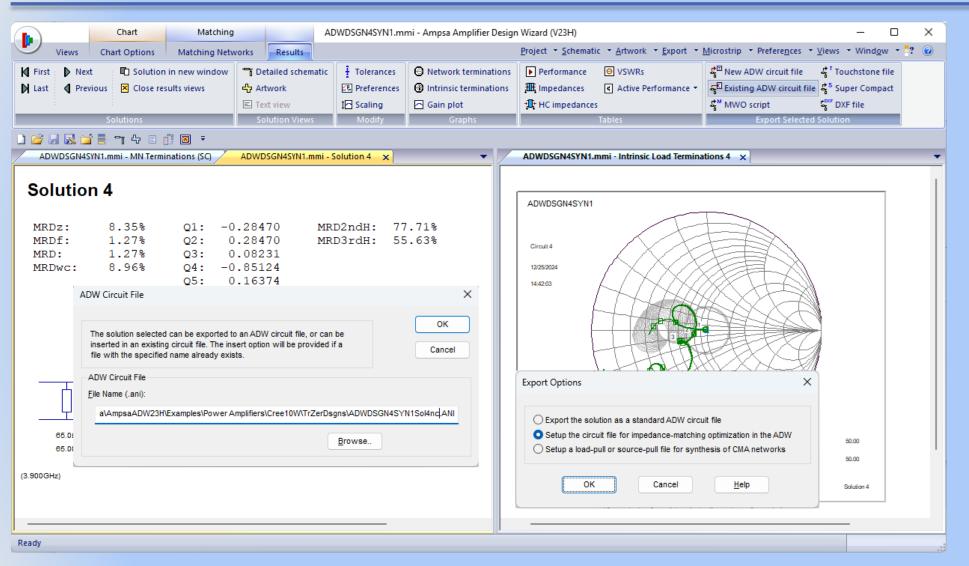




The fourth solution obtained with the tighter systematic search.

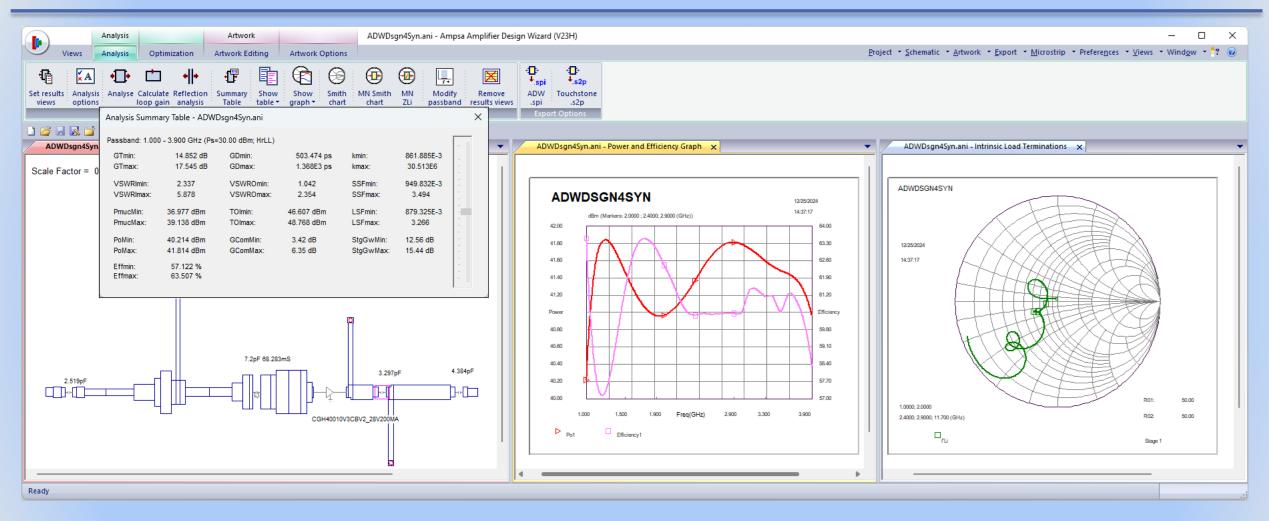
The Export Selected
Solution | Existing ADW
Circuit File option was
used to export this
solution to the original
circuit file.





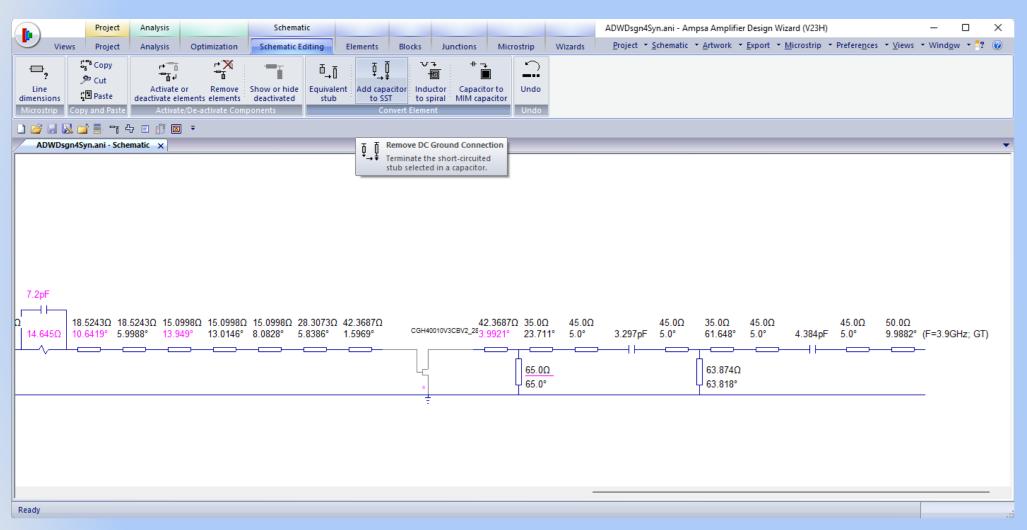
Note that new circuits can be created for any of the solutions shown. The exported matching network can then be modified or tuned or optimized before it is used in the original circuit.





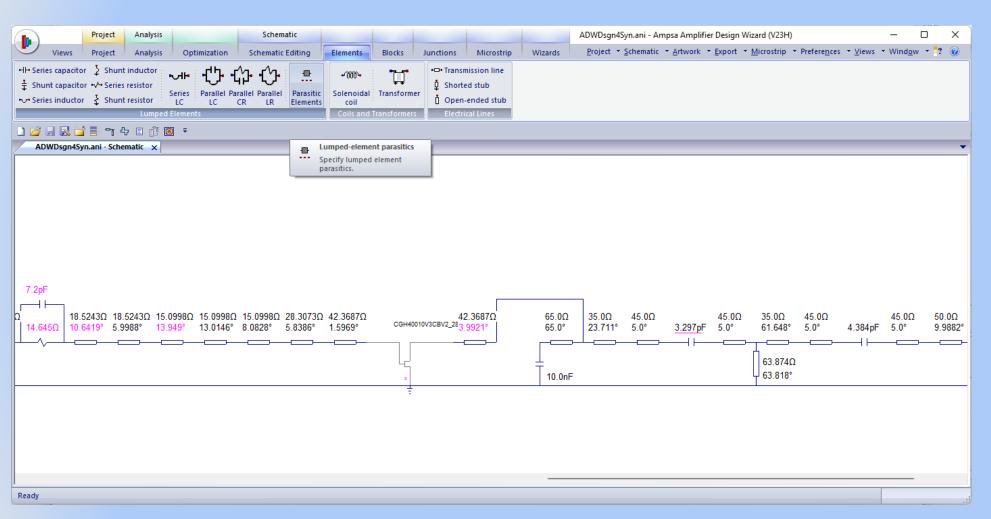
The performance obtained in the original circuit with the solution shown.





To allow for biasing the transistor, the schematic editing command shown will be used to convert the *dc* ground associated with the selected inductor to an *ac* ground.

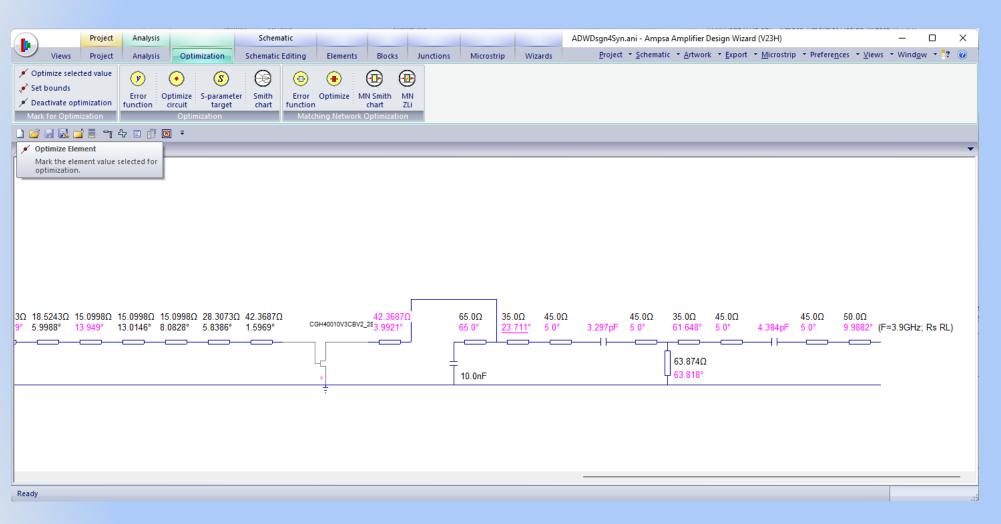




The lumped-element parasitics were ignored when this matching network was synthesized. Parasitic elements can be added to a capacitor by using the command shown after selecting the capacitor. The capacitor value can then be tuned to compensate for the inductance added.

The performance of the matching network could also be improved by tuning or optimization. To tune the network, mark all the elements in the network for optimization first.

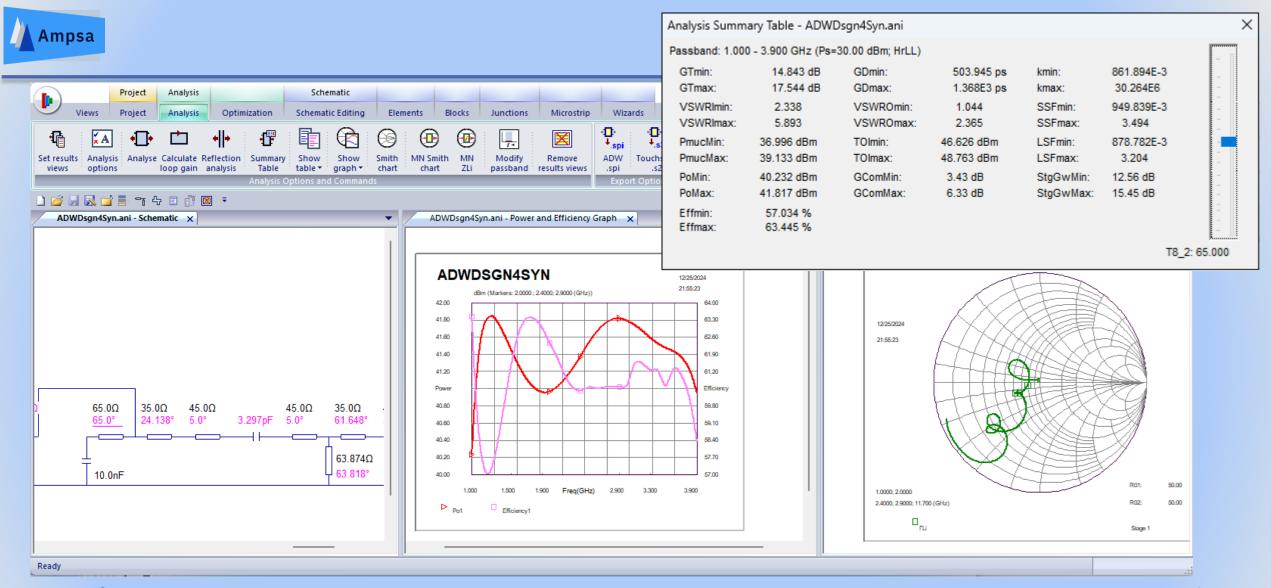




The command used to mark a variable for optimization is shown here. Note the Set Bounds command too.

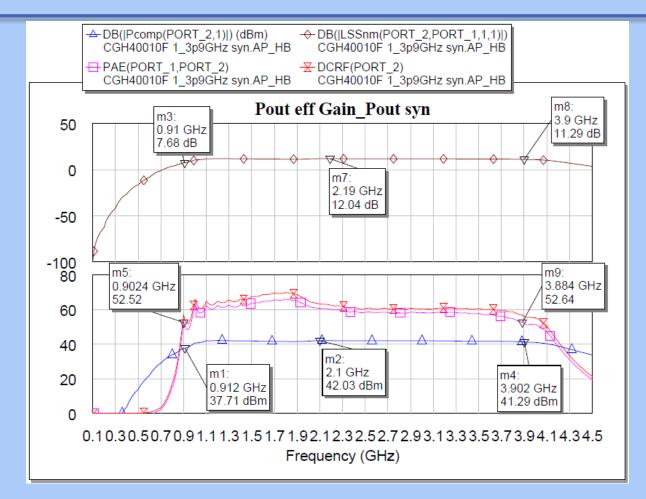
If marked for optimization, the selected variable can be tuned after selecting the Analysis | Summary Table ribbon command.

The circuit must be analysed before the element values can be tuned.



Use the Set Results Views command to set the views to be opened when an element value is tuned. The views can be arranged as required after using the Analyse command. The Summary Table command is used to tune the selected element value.

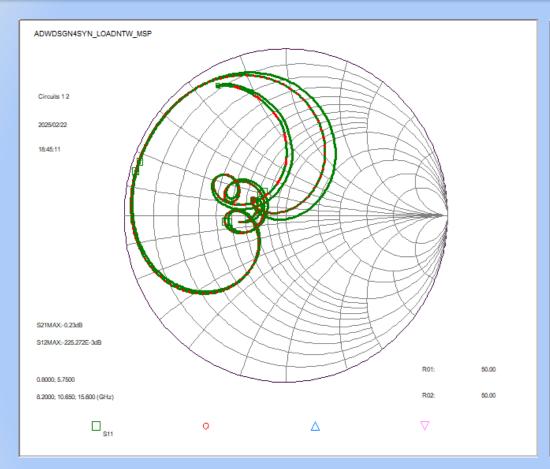






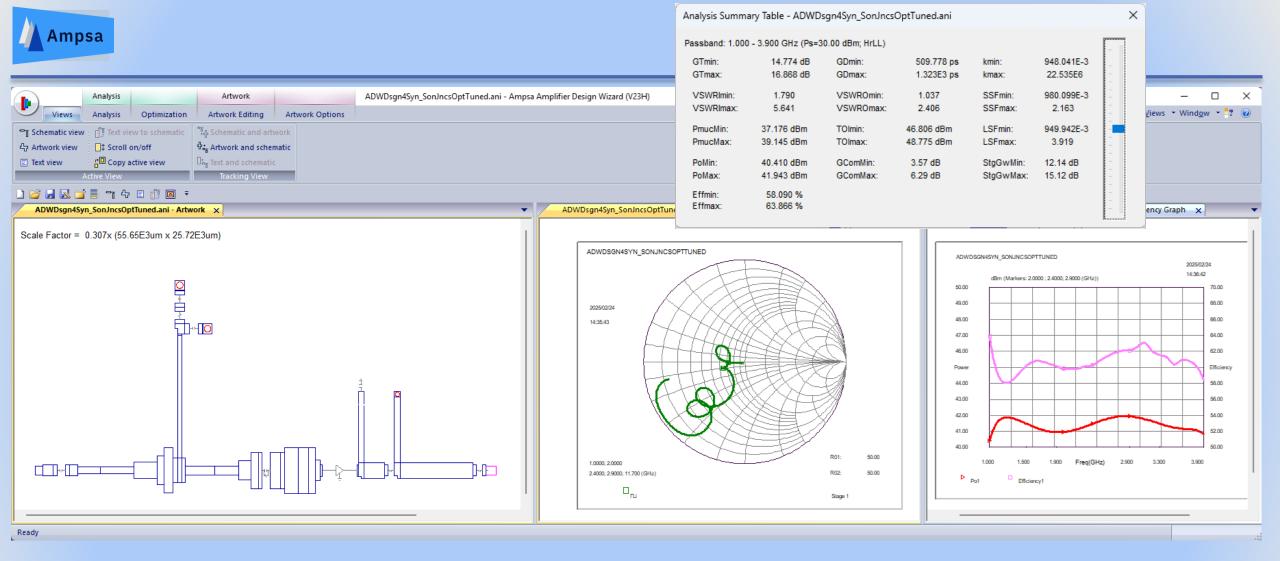
The performance of the ADW circuit in the previous slide as simulated in Microwave OfficeTM. The electrical circuit (ADW schematic) was simulated here to avoid distortions associated with differences in the microstrip models. These distortions can be reduced by using S-parameter based junctions in the ADW or by optimising the ADW microstrip networks in Microwave OfficeTM to fit the S-parameters of the ADW matching networks.







The input reflection coefficients of the load and input networks of the amplifier with implicit junctions are compared here with the reflection coefficients of these networks with S-parameter based junctions. The efficiency of the amplifier (ADW simulation) is degraded by 1% when the junctions in the load network is upgraded and by a further 1.5% when the input network is upgraded.



The performance of the amplifier with S-parameter based junctions. The input matching network was optimized first. The load network was then tuned to improve the efficiency without moving the intrinsic harmonic terminations away from Class-B operation and without losing power.