	Ampsa ADW_V23H 64-bit	Ampsa ADW_V23P 32-bit	Ampsa ADW_V23S 32-bit	Ampsa ADW_V23B 32-bit
Windows 10 / Windows 11.	Y	Y	Y	Y
Visual C++ 2022 MFC project; DPI aware up to 250DPI; ADW circuit files are Unicode text files.	Y	Y	Y	Y
Multiple documents: Ampsa circuit files (.ani); Ampsa impedance-matching data files (.mmi); Ampsa *S*-parameter data files (.spi); Ampsa transistor models are stored in .mdl files	Y	Y	Y	Y
64-bit version (Sentinel LDK hardware key protection; standalone or network options).	**Y**	**N**	**N**	**N**
Schematic views with schematic editing features. The active schematic variable can also be tuned.	Y	Y	Y	Y
Artwork views; artwork editing features.	Y	Y	Y	Y
Text editing views; text editing features.	Y	Y	Y	Y
Exporting the ADW schematic or artwork to Microwave Office™ (.bas scripts).	Y	Y	Y	Y
Exporting the ADW schematic or artwork to DXF or HPGL files. A technology file is created for exporting DXF files (artwork) to CST Microwave Studio™.	Y	Y	Y	Y
Exporting the ADW Artwork to Sonnet® Software Files (*.son).	Y	Y	Y	Y
Analysis, optimization and tuning capabilities. The active schematic variable can be tuned if marked for optimization.	Y	Y	Y	Y
Modelling of ADW microstrip steps, T-junctions and crosses with *S*-parameters obtained from an EM simulator (*S*-parameter based discontinuity models).	Y	Y	Y	Y
Nodal analysis models for square spiral inductors, parallel-plate capacitors and coupled lines.	**Y**	**Y**	**N**	**N**
Customization of microstrip discontinuity models, single-layer parallel-plate capacitor model and rectangular spiral inductor model.	**Y**	**Y**	**N**	**N**
Reflection analysis. Tuning is not allowed yet with reflection analysis.	Y	Y	Y	Y
Loop-gain analysis for an amplifier and an oscillator stage with explicit feedback. The tuning feature is active with loop gain analysis.	Y	Y	**N**	**N**
Cascade and nodal power analysis with ideal harmonic terminations assumed for the specified class of operation (ADW FFLL power analysis; extended Cripps approach). The external fundamental-frequency load terminations are mapped to the associated intrinsic fundamental-frequency load terminations by using the ADW model fitted to the transistor *S*-parameters. The allowable intrinsic load line area is defined by four or five *I*/*V*-plane boundary lines.	Y	Y	Y	Y
Power analysis with the actual harmonic terminations in place (ADW HrLL power analysis; generalized Cripps approach). The first five harmonics (fundamental included) can be controlled. Control over the assumed harmonic content is also provided. The harmonic content can also be optimized for a better fit to the simulation results obtained in a harmonic-balance simulation. The intrinsic load terminations, the dynamic load lines and the intrinsic output voltage and current waveforms can be displayed.	Y	Y	Y	**N**
Power Analysis with C_{ds} non-linear. The default C_{ds} (V_{ds}) profile used can be modified by the user.	**Y**	**Y**	**N**	**N**
Microstrip Module.	Y	Y	Y	Y
Circle Module (CIL and CIR Wizards): Constant gain (*GT*, *Ga*, *Gw*) and constant noise figure circles.	Y	Y	Y	**N**
Power Module (POW, CIL Wizard): Constant power contours can be generated for Class-A, Class-B, Class-F and Inverse Class-F amplifier stages. Maximum-Efficiency Lines can be displayed with the power contours for Class-B, Class-F and Inverse Class-F stages. Two additional constant efficiency lines can also be displayed with the maximum efficiency line (minimum efficiency targeted). Points on the contours or circular Smith Chart areas can be set automatically as fundamental-frequency impedance-matching targets. Smith chart sectors can be set as targets for the associated harmonic terminations (H2 and H3). The intrinsic and external load terminations can also be set for continuous Class-B, Class-B/J, Class-F, Inverse Class-F, and Mixed Class-F and Inverse Class-F operation. Second-harmonic clipping contours can also be generated (third and higher harmonic voltages shorted).	Y	Y	Y	**N**
Constant power contours and maximum-efficiency lines can be generated for Class-B2 stages. Control over the intrinsic load terminations of Class-B2 stages is provided.	**Y**	**Y**	**N**	**N**
Impedance-Matching Wizards (DSLT, IIM, LMT, RMT, NOI, IVI, OVI).	Y	Y	Y	Y
Synthesis of lumped-element impedance-matching networks. The element values can be constrained. The intrinsic load lines can be viewed when the matching problem was set up with the CIL Synthesis wizard. This feature is not available with license ADW_V23B.	Y	Y	Y	Y
Synthesis of non-commensurate distributed impedance-matching networks, with mixed lumped/distributed options. The characteristic impedances (line widths) are specified by the user and the line lengths are the variables. A systematic search can be done for the optimum main-line characteristic impedance. Harmonic trapping is integrated into the synthesis flow. The intrinsic load termination can be viewed when the matching problem was set up with the CIL Synthesis wizard. This feature is not available with license ADW_V23B.	Y	Y	Y	Y
Synthesis of commensurate impedance-matching networks. Different lengths are allowed for main-line elements, shorted stubs, and open stubs. The line lengths are specified by the user and the characteristic impedances (line widths) are the variables. A search can be done for the optimum main-line length. The line lengths can be set for harmonic trapping. The intrinsic load terminations can be viewed when the matching problem was set up with the CIL Synthesis Wizard. This feature is not available with license ADW_V23B.	Y	Y	Y	Y
The matching problem defined can be modified by adding fixed elements on the input and/or output sides of the networks to be synthesized.	Y	Y	Y	Y
Control over harmonic impedances when matching networks are synthesized. A Smith chart sector or a range of harmonic reactance values can be targeted at each frequency. Points, circles or circular areas can be targeted at the fundamental frequencies.	Y	Y	Y	Y
Synthesis of distributed networks (CMA networks) to control the transmission phase shift, as well as the fundamental-frequency match and the harmonic terminations. Lossless T-networks or PI-networks are synthesized. Each shunt section in the networks synthesized can consist of a single branch, two identical branches in parallel or a resonating section. Pads are allowed for the lumped components. The synthesis is exact at a selected passband frequency. A systematic search on the design space is done for the best broadband solutions (best match). If a specific phase shift is required, the phase can be fixed when the systematic search is done.	Y	Y	Y	Y
Modification and optimization of a synthesized matching network in the Analysis module. The error function used for optimization can be similar to that used during synthesis.	Y	Y	Y	Y
The DSLT synthesis wizard can be used to synthesize the (even-mode) branches of a Wilkinson splitter. The splitter performance can be optimized by optimizing *s*11 and *s*21 of the even mode and *s*22 of the odd mode. The nodal dual-state analysis command (NDST) can be used to analyse and optimise the splitter in the ADW. NDST commands can also be used to analyse and optimize three-port splitters with different power levels and/or phases at the output ports.	Y	Y	Y	Y
S-parameter Module; Specifying or fitting small-signal transistor models (Class-A, Class-B, Class-F, and Inverse Class-F). The class of operation can be set with the associated harmonic content.	Y	Y	Y	**N**
S-parameter Module: Class-B2 features.	**Y**	**Y**	**N**	**N**
S-parameter Module: Modification network synthesis (resistive feedback and loading networks).	Y	Y	**N**	**N**
User guides (pdf format).	Y	Y	Y	Y
Permanent Licenses (Sentinel LDK hardware keys)				
Standalone single-user license fee	$7 500	$7 000	$4 900	$3 300
License fee for additional users	$5 625	$5 250	$3 675	$2 475
Annual support/upgrade fee (single user; optional)	$1 125	$1 050	$735	$ 495
Network license fee (one user at a time)	$11 250	$10 500	$7 350	$4 950
License fee for each concurrent user	$9 000	$8 400	$5 880	$3 960
Annual support/upgrade fee (one user at a time; optional)	$1 685	$1 575	$1100	$740
Subscription Licenses				
Sixty days (60 days) subscription standalone single-user license (software-based protection)		$450	$325	$250
Annual subscription standalone single-user license (software-based protection)		$2 300	$1 650	$1 250
Annual subscription network license (Concurrency: 1)		$3 300	$2 400	$1 900

Support and upgrades are provided free of charge for the first two months after obtaining a new permanent license. A subscription license can be renewed annually and include upgrades and support while the license is active.

University License:
Only subscription licenses are available for educational purposes. A discount of 40% is provided on the subscription license fees listed.
A University license is issued for educational or research purposes only. Contract work is not allowed.

All license fees are listed in **US dollars**. Payment is required by wire transfer, direct deposit or by credit card (https://www.ampsa.com).

1-February-2025

Introduction to the Ampsa Amplifier Design Wizard

The Ampsa Amplifier Design Wizard (ADW) is a synthesis tool. A harmonic-balance simulator is required to verify and optimize the performance of an amplifier designed in the ADW. Ideally the difference between the performance obtained in the ADW and that obtained in the harmonic-balance simulator should be minor. Considerable effort went into the development of the ADW to minimize the discrepancies.

The ADW load-pull and analysis (optimization) capabilities are based on clipping theory. (Clipping of the intrinsic load line on the *I*/*V*-plane boundaries defined.) Clipping theory provides a bridge between linear analysis and harmonic-balance analysis.

Clipping theory has been developed to a fully useful point in the ADW: The load terminations presented by a matching network are mapped automatically to the intrinsic reference plane of the transistor by using power parameters and the harmonic content is estimated from continuous mode theory for the assumed class of operation. The classes allowed in the ADW are Class-A, class-B (including class-AB), class-F, inverse class-F and class-B2. The associated continuous modes are also allowed. Note that the output driving waveform is half-sinusoidal (or approximate half-sinusoidal) current for class-B and class-F, and a half-sinusoidal (or approximate half-sinusoidal) voltage for inverse class-F and class-B2; class B2 stands to inverse class-F as class-B stands to class-F.

Extensive control over the assumed harmonic content is provided in the ADW. Up to five harmonics are considered. Search and optimization features for the assumed harmonic content are also provided to improve the fit of the performance obtained in the ADW with that obtained in a harmonic-balance simulation or in actual measurements (that is, if necessary).

With the intrinsic load terminations calculated and the harmonic content estimated, the dynamic intrinsic load lines can be plotted in the ADW. Four or five boundary lines is used to define boundaries for the dynamic load lines in the intrinsic *I*/*V*-plane. The fifth boundary is used to model the upper-left corner in the transistor knee. Hard clipping on one of the boundaries is assumed. (The power at clipping is the maximum unclipped output power (P_{muc}); note that P_{muc} does not depend on the input match.) A compression curve is used for power levels above or below P_{muc}.

Except for the output capacitance (C_{ds}), the components in the transistor model are assumed to be linear. (The required models can be fitted in the ADW.) The default capacitance versus voltage profile used for C_{ds} can be modified by the user.

Continuous-mode theory or the fundamental-frequency load terminations with ideal harmonic terminations for the specified class of operation (FFLL) are used during synthesis. When the designed circuit is analysed or optimized in the ADW, the option to use the actual terminations presented by the matching network (HrLL) is provided. When the HrLL option is used, C_{ds} can be set to be constant or to have the non-linear $C(V)$ profile specified. Fourier analysis is used to calculate the harmonic components of the current in C_{ds}.

Analysis Module

Schematic views, artwork views, as well as text views are provided in the ADW Analysis module. Editing features are provided in all the views.

If marked for optimization, the selected element value in a schematic view can be tuned by opening the summary table provided when the circuit is analysed. The optimization bounds set for the value is used to set the tuning range but can be overridden.

Some of the capabilities provided in the ADW analysis module are:

- *S*-parameter analysis.
- Power and efficiency analysis (ADW cascade circuits).
- Stability analysis. This includes loop-gain analysis for an amplifier or oscillator stage.
- Reflection analysis at cascade positions in the circuit.
- Differences in the microstrip models used in the ADW and the harmonic-balance simulator can cause discrepancies in the performance. Instead of using the standard ADW discontinuity models, the parameters of more sophisticated models can be fitted to *S*-parameters obtained in EM simulations, or the discontinuity *S*-parameters can be used directly (recommended). *S*-parameter based models for steps, T-junctions and crosses are provided in the ADW. Note that it always a good idea to export the electrical ADW circuit (not the microstrip circuit) to the harmonic-balance simulator in the initial stages of a design cycle – The ADW design can then be verified without the complications of the microstrip models. When the EM-based *S*-parameters for the junctions are in place in the ADW, the performance can be restored in the ADW by optimization, and the optimized artwork can then be exported.
- The ADW electrical circuit or the artwork can be exported to Microwave Office™, and the artwork can be exported to Sonnet Software®'s EM. The artwork can also be exported to ADS™ for use in Momentum™ via DXF files. The electrical circuit cannot be exported to ADS™, but an alternative to manually entering the electrical circuit is to use the *S*-parameters for each ADW matching network in ADS for the verification.
- Wizards (CIL, CIR, IIM, IVI, OVI, POW) are provided to set up a variety of impedance-matching problems. These problems are then solved by using the ADW Impedance-Matching Module or the CMA wizard.
- Synthesis (CMA wizard) of distributed T-networks or PI-networks (parallel sections or resonating sections are allowed in the shunt positions of these networks) to control the transmission phase shift, as well as the match. The synthesis is exact at the passband frequency selected. A systematic search on the design space is done for the best broadband solutions.
- Optimization and tuning of passive circuits or designed amplifiers. The intrinsic load terminations can also be optimized.

ADW Synthesis Capabilities

1. The microstrip module provided can be used to calculate the dimensions for an electrical line or the electrical characteristics of a microstrip line.

2. Constant-gain (G_T, G_a, G_ω) and constant noise figure circles can be plotted in the CIL and CIR Wizards.

3. Constant-power contours and maximum-efficiency lines for Class-A, Class-B, Class-F, Inverse Class-F and class-B2 amplifier stages can be plotted with the CIL Wizard. Points or circular Smith Chart areas can be set automatically as impedance-matching targets. Smith chart sectors can be set as targets for the second and third harmonic frequencies.

4. Second-harmonic clipping contours (third and higher harmonic voltages assumed to be shorted) can be plotted for the optimum class-B terminations or any fundamental-frequency termination selected in the power contour section.

5. Extensive impedance-matching capabilities are provided in the Impedance-Matching module.

   At the fundamental frequencies, the targets can be points or circular areas. (The circumference or the inside or outside of a circle can be targeted.) At a harmonic frequency (second and/or third harmonic), the target can be a range of reactance values, or a sector defined by a local origin inside the Smith Chart and two points on the edge of the chart.

   A matching problem can be modified by adding fixed elements on the input and/or output side of the networks to be synthesized.

   A systematic search can be done to find the optimum main-line length for commensurate solutions. In non-commensurate solutions, the search is done on the characteristic impedance of the main-line sections.

   Harmonic trapping is integrated into the synthesis algorithm for non-commensurate matching networks. Different trap frequencies can be specified for the open-ended branches and the shorted branches in the network. The trap frequency for shorted branches must be lower or equal to that for open-ended branches.

   Parasitic inductance or capacitance can be added to lumped capacitors or inductors, respectively. The parasitic element can have a fixed value or can be used for harmonic trapping. Different trap frequencies can be specified for the capacitors and the inductors.

   When the CIL wizard was used to setup the matching problem, the intrinsic harmonic load terminations can be used as targets instead of the associated external terminations. Better results are obtained when this is done.

6. Modification networks (lossy sections added to the transistor; feedback or loading sections) can be synthesized to stabilize a transistor, to level the power gain and to improve the input and/or the output VSWRs before matching.

Transistor Modelling Capabilities

Linear bipolar or FET/HEMT transistor models can be fitted to a set of wideband *S*-parameters in the ADW. (The standard fitting procedure usually yields a tight fit in the parameters.) The boundary constraints on the intrinsic load-line can be obtained from *dc* or pulsed *I*/*V*-curves. The harmonic content for the different classes of operation is estimated from continuous-mode theory and can be adjusted by the user. The class of operation can be fixed for a model, or mode-switching can be allowed.

The model parameters can be adjusted to improve the fit with the information (gain, power, and optimum terminations) provided in the datasheet or harmonic-balance simulation of a test circuit. These adjustments can be manual or by using the optimization features provided for this purpose.

Export Capabilities

ADW circuits can be exported in various formats:

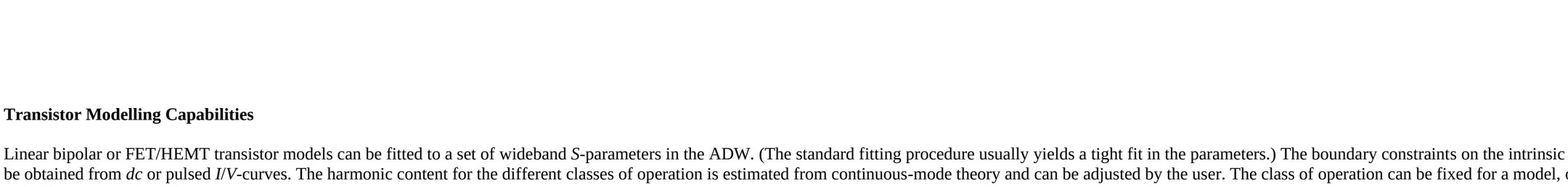
- The schematic or artwork can be exported to Microwave Office™ as a basic script (.bas file).
- The schematic or artwork can be exported in HPGL or DXF format. A technology file can also be created for CST Microwave Studio™ when the artwork is exported in DXF format.
- The artwork can be exported as a Sonnet® Software files (*.son).
- The artwork can be exported to Momentum™ in DXF format.

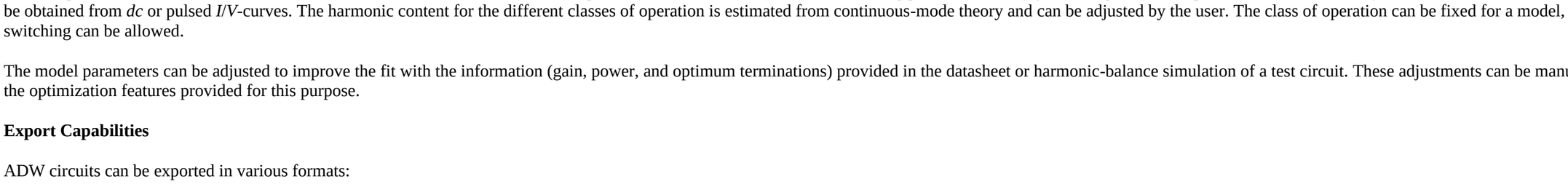
ADW Ribbon Categories

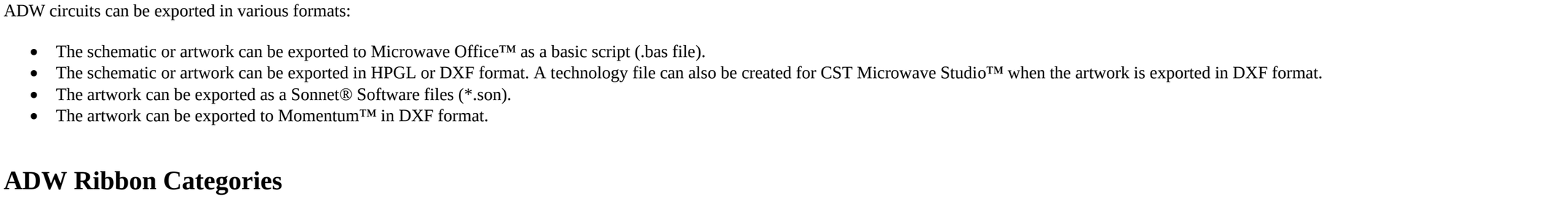
The ribbon categories and the ribbon commands provided in the Amplifier Design Wizard are shown here to provide an overview to the capabilities provided in the ADW.

Analysis Module

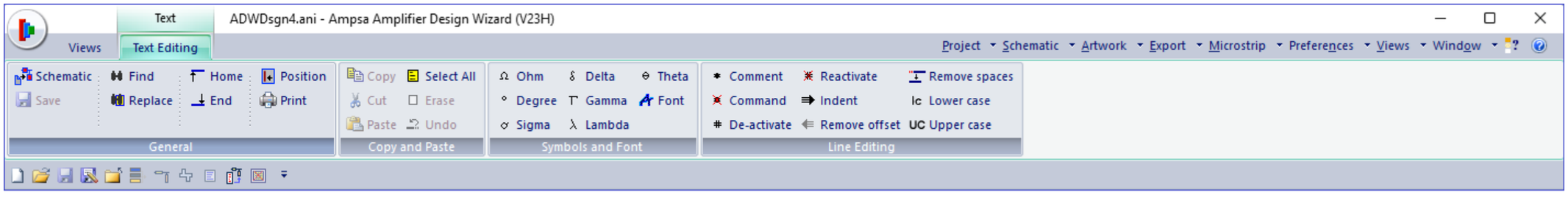
View, Project, Analysis and Optimization Categories



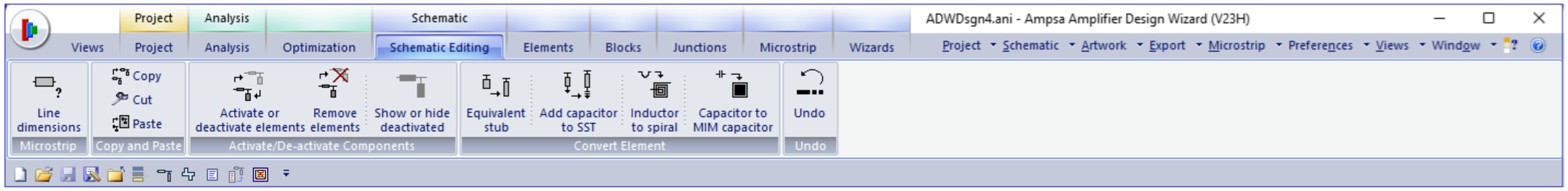


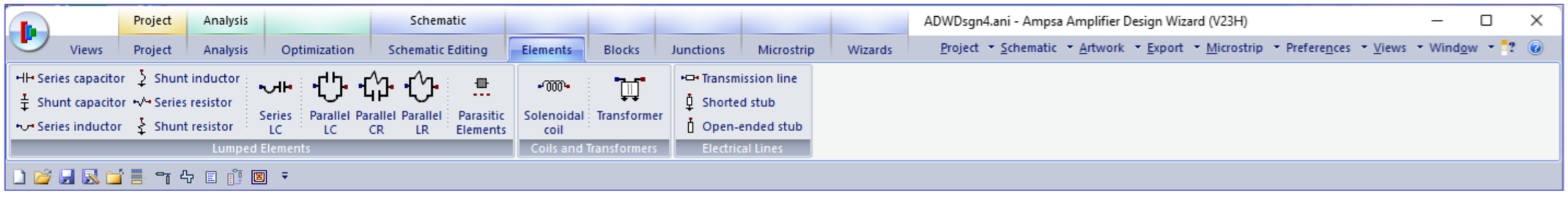


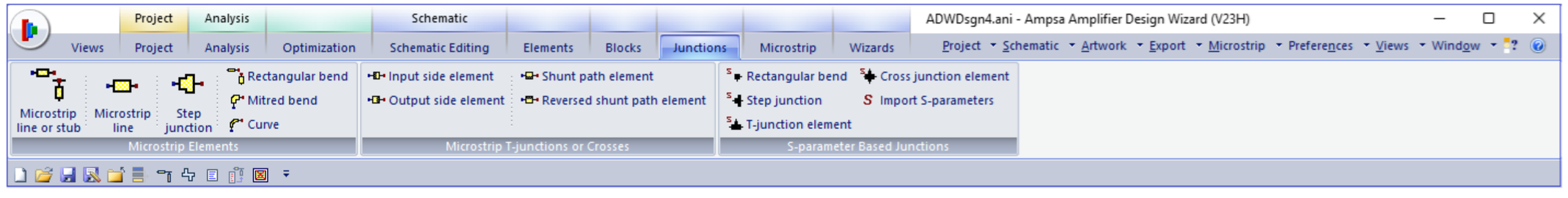
Text Editing Ribbon

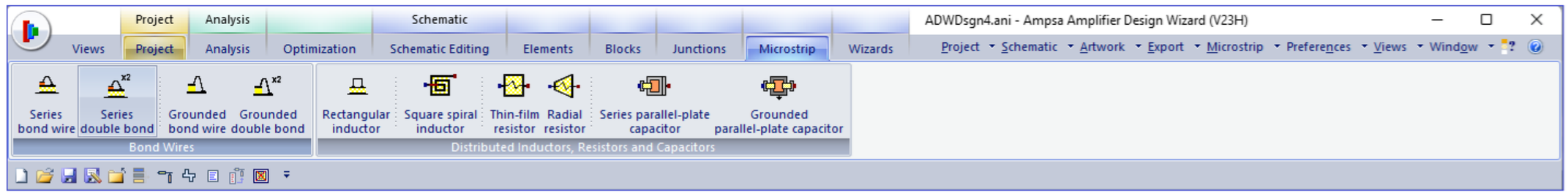


Schematic Editing Ribbons

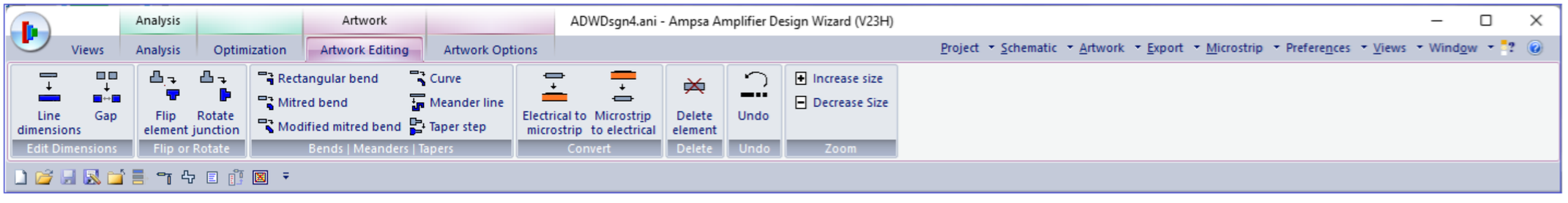


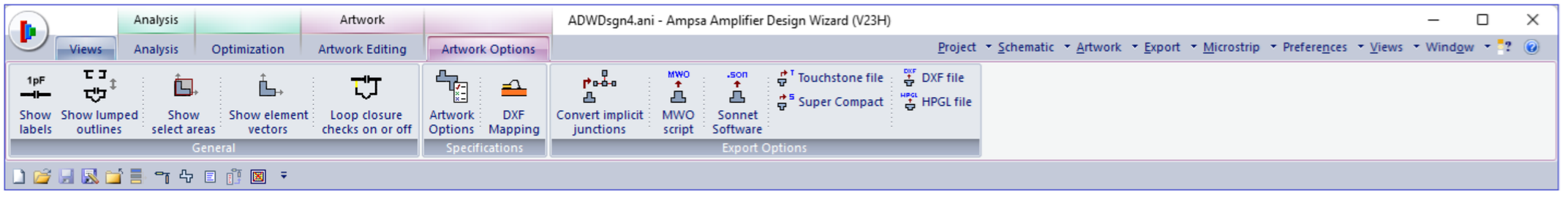




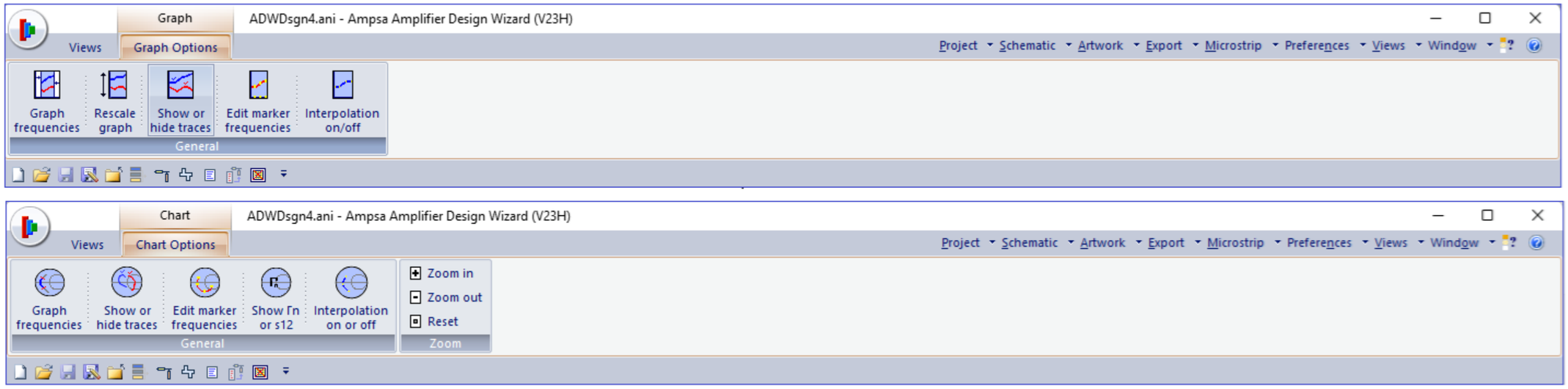


Artwork Editing Ribbons

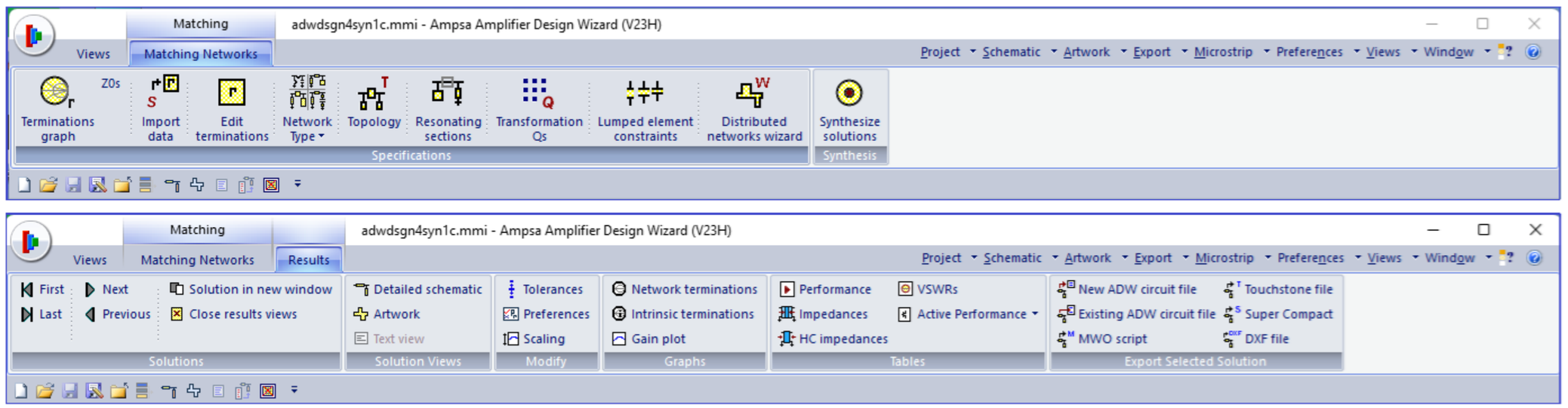




Rectangular Plot and Smith Chart Categories



Impedance-Matching Module



S-parameter Module